

	NN	NN		AAAAAA	DDDDDDDD	PPPPPPPP	77777777	5555555555	000000	000000
	NN	NN		AAAAAA	DDDDDDDD	PPPPPPPP	77777777	5555555555	00	00
	NN	NN		AA	AA	DD	DD	55	00	00
	NN	NN		AA	AA	DD	DD	55	00	00
	NNNN	NN		AA	AA	DD	DD	55	00	00
	NNNN	NN		AA	AA	DD	DD	55	00	00
	NN NN	NN		AA	AA	DD	DD	55	00	00
	NN NN	NN		AA	AA	DD	DD	55	00	00
	NN NNNN	NN		AAAAAA	DD	DD	PP	77	00	00
	NN NNNN	NN		AAAAAA	DD	DD	PP	77	00	00
	NN NN	NN		AA	AA	DD	DD	55	00	00
	NN NN	NN		AA	AA	DD	DD	55	00	00
	NN NN	NN		AA	AA	DDDDDDDD	PP	77	000000	000000
	NN NN	NN		AA	AA	DDDDDDDD	PP	77	000000	000000
LL		SSSSSSSS	SSSSSSSS					
LL		SS	SS							
LL		SS	SS							
LL		SSSSSS	SSSSSS							
LL		SSSSSS	SSSSSS							
LL		SS	SS							
LL		SS	SS							
LL		SSSSSSSS	SSSSSSSS							
LL		SSSSSSSS	SSSSSSSS							

(3)	254	Macros to describe nexus configurations
(4)	379	Adapter-specific data structures
(5)	523	CPU-specific data structures
(6)	723	Message strings
(7)	734	INI\$IONMAP Initialize and map nexuses
(8)	899	INITADP 780, 750, -730, and _UV1
(9)	916	CONFIG_IOSPACE
(10)	1066	CREATE-ARRAYS
(11)	1109	MAP PAGES
(13)	1269	INI\$SUBSPACE
(14)	1539	INI\$UBADP - BUILD ADP AND INITIALIZE UBA
(14)	1815	INI\$MBADP - BUILD ADP AND INITIALIZE MBA
(14)	1816	INI\$DRADP - BUILD ADP AND INITIALIZE DR32
(14)	1817	INI\$CIADP - BUILD ADP AND INITIALIZE CI
(14)	1997	INI\$KDZ11
(14)	2031	INI\$CONSOLE, init data structures for console
(15)	2141	EXE\$INI_TIMWAIT - COMPUTE CORRECT TIMEWAIT LOOP VALUES
(16)	2299	EXE\$INIT_TODR - SET SYSTEM TIME TO CORRECT VALUE AT STARTUP

```
0000 1 .NLIST CND
0000 5
0000 7
0000 9
0000 13
0000 17
0000 21
0000 25
0000 26 .IDENT 'V04-002'
0000 27
0000 28 ****
0000 29 *
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0000 46 * SOFTWARE ON EQUIPMENT WHICH IS NOT SUPPLIED BY DIGITAL.
0000 47 *
0000 48 *
0000 49 ****
0000 50
0000 51 Facility: System bootstrapping and initialization
0000 52
0000 53 Abstract: This module contains initialization routines that are loaded
0000 54 during system initialization (rather than linked into the system).
0000 55
0000 56 Environment: Mode = KERNEL, Executing on INTERRUPT stack, IPL=31
0000 57
0000 58 Author: Trudy C. Matthews Creation date: 22-Jan-1981
0000 59
0000 60 Modification history:
0000 61
0000 62 V04-002 TCM0013 Trudy C. Matthews 10-Sep-1984
0000 63 Add $BQODEF missing from TCM0012.
0000 64
0000 65 V04-001 TCM0012 Trudy C. Matthews 07-Sep-1984
0000 66 For venus processor: turn on cache before calibrating
0000 67 TIMEDWAIT cells (routine EX$INI_TIMWAIT). Store the TIMEDWAIT
0000 68 values calculated after cache is enabled in the boot driver's
0000 69 TIMEDWAIT cells. This is because the boot driver initially
0000 70 has to run with cache off, but after booting will run with
0000 71 cache on.
0000 72
0000 73 V03-024 TCM0011 Trudy C. Matthews 31-Jul-1984
0000 74 Change venus's CRD interrupt vector back to ^X54 in the SCB.
```

0000 75 and its SBIA Fail vector to "X64.
 0000 76
 0000 77
 0000 78 V03-023 WMC0001 Wayne Cardoza 30-Jul-1984
 0000 79 Add H memory to 780 list.
 0000 80
 0000 81 V03-022 TCM0010 Trudy C. Matthews 25-Jul-1984
 0000 82 Fix a bug in INI\$SUBSPACE for the 11/790 that caused second
 0000 83 and subsequent unibus adapter spaces to be mapped incorrectly.
 0000 84 Fix bugs in INI\$SCB for the 11/790. Fix conditional
 0000 85 assembly flags in INI\$CONSOLE for the 11/790.
 0000 86 V03-021 KDM0100 Kathleen D. Morse 01-May-1984
 0000 87 Correct address of memory [SRs to be past the 8 missing
 0000 88 Qbus adapter pages that do not exist.
 0000 89
 0000 90 V03-020 KDM0099 Kathleen D. Morse 27-Apr-1984
 0000 91 On a MicroVAX I, if the sysgen parameter TIMEDWAIT is set
 0000 92 to request no time-prompting, then use the last recorded
 0000 93 system time instead. This is found in EXESGQ_TODCBASE
 0000 94 which can be updated with a SET TIME command.
 0000 95
 0000 96 V03-019 RLRSCORPIO Robert L. Rappaport 16-Mar-1984
 0000 97 Begin additions (to INI\$IOMAP) for Scorpio support.
 0000 98 Also move ADAPDESC to SYSMAR.MAR, changing it to remove
 0000 99 the ADAP_GENERAL array.
 0000 100
 0000 101 V03-018 RLRINIADP Robert Rappaport 28-Feb-1984
 0000 102 Add refinements to previous update that introduces
 0000 103 longword array CONFREG. Mainly add logic to allow for
 0000 104 independently assembled invocations of ADAPDESC macro
 0000 105 to be linked into this code. This provides possible
 0000 106 support of BI as a public bus, with user defined nodes.
 0000 107
 0000 108 V03-017 KPL0100 Peter Lieberwirth 30-Jan-1984
 0000 109 Implement first step towards a longword-array CONFREG to
 0000 110 replace current byte array CONFREG. INIADP will construct
 0000 111 two confregs, CONFREG and CONFREGL. CONFREGL will be
 0000 112 a longword array. The high byte will be a VMS-bus
 0000 113 designation, and the low word will contain the 16-bit
 0000 114 device type. The BI introduces 16 bit device types.
 0000 115
 0000 116 When all references to CONFREG have been modified to touch
 0000 117 CONFREGL, INIADP will be modified again to stop creating
 0000 118 the byte array.
 0000 119
 0000 120 While here, map 9 pages of CI register space, up from 8.
 0000 121
 0000 122 V03-016 KPL0001 Peter Lieberwirth 17-Jan-1984
 0000 123 Fix bug in V03-015 that caused a failure to boot on 750s.
 0000 124 Specifically, add NDT\$_MEM1664NI to ADAPDESC macro.
 0000 125
 0000 126 V03-015 TCM0009 Trudy C. Matthews 12-Dec-1983
 0000 127 Add support for booting from VENUS console device to
 0000 128 INI\$CONSOLE. When mapping I/O space on VENUS, use the
 0000 129 PAMM to determine if any adaptors are present on the
 0000 130 ABUS.
 0000 131

0000	132	V03-014	KDM0081	Kathleen D. Morse	13-Sep-1983
				Create version for Micro-VAX I.	
0000	133	V03-013	DWT0126	David W. Thiel	30-Aug-1983
				Modify EXE\$INIT_TODR to set internal time without	
0000	134			modifying the contents of the system disk.	
0000	135	V03-012	KDM0062	Kathleen D. Morse	18-Jul-1983
				Add loadable, cpu-dependent routine for initializing	
0000	136			the time-wait loop data cells, EXE\$INI_TIMWAIT.	
0000	137	V03-011	KDM0057	Kathleen D. Morse	15-Jul-1983
				Added loadable, cpu-dependent routine for initializing	
0000	138			the system time, EXE\$INIT_TODR.	
0000	139	V03-010	KTA3071	Kerbey T. Altmann	12-Jul-1983
				Include CPU-specific console init code.	
0000	140	V03-009	TCM0008	Trudy C. Matthews	10-Jan-1983
				Change PSECT of 11/790 data that must stick around after	
0000	141			INIADP is deleted. Build arrays ABUS_VA, ABUS_TYPE, and	
0000	142			ABUS_INDEX that describe the 11/790 ABUS configuration.	
0000	143	V03-008	MSH0002	Maryann Hinden	08-Dec-1982
				Add powerfail support for DW750.	
0000	144	V03-007	ROW0142	Ralph O. Weber	24-NOV-1982
				Change UBA interrupt services routines prototype so that	
0000	145			UBAERRADDR is correctly computed as an offset from UBAINTBASE.	
0000	146	V03-006	TCM0007	Trudy C. Matthews	10-Nov-1982
				Add 11/790-specific initialization of SCB.	
0000	147	V03-005	TCM0006	Trudy C. Matthews	8-Nov-1982
				Initialize field ADPSL_AVECTOR with the address of	
0000	148			each adapter's first SCB vector.	
0000	149	V03-004	KTA3018	Kerbey T. Altmann	30-Oct-1982
				Move from INILOA facility, rename from INITADP,	
0000	150			put in conditional assembly, rewrite some routines.	
0000	151	V03-003	MSH0001	Maryann Hinden	24-Sep-1982
				Change EXESDW780_INT to EXESUBAERR_INT.	
0000	152	V03-002	TCM0005	Trudy C. Matthews	10-Aug-1982
				Added support for 11/790 processor.	
0000	153	V03-001	KDM0002	Kathleen D. Morse	28-Jun-1982
				Added \$DCDEF.	
0000	154				
0000	155				
0000	156				
0000	157				
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0000	159				
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0000	177				
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0000	179				
0000	180				
0000	181				
0000	182	--			

0000	184	
0000	185	; MACRO LIBRARY CALLS
0000	186	
0000	187	\$ADPDEF
0000	188	\$BIICDEF
0000	189	\$BQODEF
0000	190	\$BTDDDEF
0000	191	\$BUADEF
0000	192	\$CRBDEF
0000	193	\$DCDEF
0000	194	\$DDBDEF
0000	195	\$DYNDEF
0000	196	\$IDBDEF
0000	198	\$I0750DEF
0000	199	\$UASDEF
0000	219	\$MCHKDEF
0000	220	\$SNDTDEF
0000	221	\$PRDEF
0000	222	
0000	226	
0000	228	SPR750DEF
0000	230	
0000	234	
0000	238	
0000	242	
0000	246	
0000	247	\$PTEDEF
0000	248	\$RPBDEF
0000	249	\$UBADEF
0000	250	\$UCBDEF
0000	251	\$VADEF
0000	252	\$VECDEF

; Define ADP offsets.
; Define BIIC offsets.
; Define boot vector offsets.
; Define boot devices
; Define BUA Register offsets.
; Define CRB offsets.
; Define adapter types
; Define DDB offsets
; Define data structure type codes.
; Define interrupt dispatcher offsets.
; Define 11/750 I/O space.
; Define DW750 IPEC registers.
; Define machine check masks.
; Define nexus device types.
; Define IPR numbers.

; Define 11/750 specific IPR numbers.

; Define Page Table Entry bits.
; Define Restart Parameter Block fields.
; Define UBA register offsets.
; Define UCB offsets.
; Define virtual address fields.
; Define vec offsets.

0000 254 .SBTTL Macros to describe nexus configurations
0000 255 :
0000 256 The macros FLOAT_NEXUS and FIXED_NEXUS add one or more entries to a
0000 257 nexus descriptor table. Each entry is of the form:
0000 258 +-----+
0000 259 | PFN of nexus I/O space |
0000 260 +-----+ +-----+
0000 261 | bus | 0 | type |
0000 262 +-----+ +-----+
0000 263 type = 0 -> floating nexus
0000 264 type = non-zero -> fixed nexus; type = fixed adapter type
0000 265 bus = 0, if SBI; %x80 if BI (this is a VMS-only designation)
0000 266 :
0000 267 :
0000 268 device_type: SBI adapters have 8-bit device type codes. These
0000 269 device types are simple integers.
0000 270 :
0000 271 BI adapters have 16-bit device type codes, that are
0000 272 subject to the following interpretation:
0000 273 :
0000 274 - the MSB of the device-type field will be 0 for DEC
0000 275 devices and 1 for non-DEC devices.
0000 276 :
0000 277 - DEC memory devices will have 0s in the high-order
0000 278 byte of the device type.
0000 279 :
0000 280 - non-DEC supplied memory devices will have a 1 in the
0000 281 MSB of the high-order byte, and the rest of the high
0000 282 order byte will contain 0s.
0000 283 :
0000 284 - The "all 0s" and "all 1s" device-type codes are
0000 285 reserved for DEC.
0000 286 :
0000 287 If SBI type codes were simply expanded to a word for purposes of the routines
0000 288 in this module, there would be possible conflicts between SBI devices and
0000 289 BI memory adapters supplied by DEC. Voila: the bus type.
0000 290 :
0000 291 Macro FLOAT_NEXUS.
0000 292 INPUTS:
0000 293 PHYSADR -- physical address of 1 or more contiguous floating nexus
0000 294 slots
0000 295 :
0000 296 NUMNEX -- number of contiguous floating nexuses, default = 1
0000 297 PERNEX -- amount of address space per nexus (does not have to be
0000 298 specified if NUMNEX = 1)
0000 299 :
0000 300 .MACRO FLOAT_NEXUS PHYSADR,NUMNEX=1,PERNEX=0
0000 301 PA = PHYSADR : For each nexus...
0000 302 .REPEAT NUMNEX : Store PFN.
0000 303 .LONG <PA/^X200>
0000 304 .LONG 0 : Store floating nexus type.
0000 305 PA = PA + PERNEX : Increment to physical address of next nexus.
0000 306 .ENDR :
0000 307 .ENDM FLOAT_NEXUS :
0000 308 :
0000 309 : Macro FIXED_NEXUS.
0000 310 :
0000 311 :

```

0000 311 : INPUTS:
0000 312 : PHYSADR - physical address of 1 or more contiguous fixed nexus slots
0000 313 : PERNEX - amount of address space per nexus
0000 314 : NEXUSTYPES - a list of fixed nexus types, enclosed in <>
0000 315 :
0000 316 : MACRO FIXED_NEXUS PHYSADR,PERNEX=0,NEXUSTYPES
0000 317 : PA = PHYSADR
0000 318 : .IRP TYPECODE,NEXUSTYPES : For each fixed nexus type...
0000 319 : .LONG <PA/^X200> : Store PFN.
0000 320 : .LONG TYPECODE : Store fixed nexus type.
0000 321 : PA = PA + PERNEX : Increment to address of next nexus.
0000 322 : .ENDR
0000 323 : .ENDM FIXED_NEXUS
0000 324 :
0000 325 :
0000 326 : Macro NEXUSDESC_TABLE - declare the beginning of a NEXUS descriptor table
0000 327 :
0000 328 : 1st byte in table (at offset -5 from label) contains length of
0000 329 : adapter type code field in CSR's on this bus. [Note for SBI like
0000 330 : busses, this is 1.] The next longword (at offset -4) in the
0000 331 : table contains the Software defined bus type byte defined in the
0000 332 : high order byte of the longword. [Note for SBI like busses, this
0000 333 : value is 0, for the BI it is ^X80.]
0000 334 :
0000 335 :
0000 336 : Define parameters that may be specified or used in macro invocation.
0000 337 :
0000 338 :00000000 BI_LIKE = 0 ; BI like bus.
0000 339 :00000001 SBI_LIKE = 1 ; SBI like bus.
0000 340 :
0000 341 :00000001 SBI_CSR_LEN = 1 ; Length of type code field in adapter CSR's
0000 342 : on SBI, CMI, etc.
0000 343 :00000002 BI_CSR_LEN = 2 ; Length of type code field in adapter CSR's
0000 344 : on BI.
0000 345 :
0000 346 :00000000 SBI_BUS_CODE = 0 ; Software defined bus code for SBI like busses.
0000 347 :80000000 BI_BUS_CODE = ^X80000000 ; Software defined bus code for the BI.
0000 348 :
0000 349 : .MACRO NEXUSDESC_TABLE LABEL,BUS_TYPE=SBI_LIKE
0000 350 : .IF EQ,BUS_TYPE-SBI_LIKE
0000 351 : .BYTE SBI_CSR_LEN
0000 352 : .LONG SBI_BUS_CODE
0000 353 : .IFF
0000 354 : .IF EQ,BUS_TYPE-BI_LIKE
0000 355 : .BYTE BI_CSR_LEN
0000 356 : .LONG BI_BUS_CODE
0000 357 : .IFF
0000 358 : .ERROR : UNRECOGNIZED BUS TYPE, NEXUSDESC_TABLE;
0000 359 : .ENDC
0000 360 : .ENDC
0000 361 :
0000 362 : LABEL:
0000 363 : .ENDM NEXUSDESC_TABLE
0000 364 :
0000 365 :FFFFFB CSR_LEN_OFFSET = -5 ; Offset before nexus descriptor of
0000 366 : byte containing length of adapter
0000 367 : type field in adapter CSR.

```

```
FFFFFFFC 0000 368 BUS_CODE_OFFSET = -4 ; Offset before nexus descriptor table
0000 369 ; of longword containing software
0000 370 ; defined bus type to be or'ed with
0000 371 ; adapter type to produce NDT$_ value.
0000 372
0000 373 ; Macro END_NEXUSDESC.
0000 374 ; .MACRO END_NEXUSDESC
0000 375 .LONG 0
0000 376 .ENDM END_NEXUSDESC ; PFN=0 -> end of nexus descriptors.
0000 377
```

```

0000 379 .SBTTL Adapter-specific data structures
0000 380
0000 381 ; Put a symbol for arrays built by macros in the correct psects.
0000 382
0000 383 ;***** ADAPTERS array *****
0000 384 .PSECT $SSINIT$DATA0
0000 385 ADAPTERS: ; Build adapter type code arrays here.
0000 386
0000 387 .PSECT $SSINIT$DATA1 ; User contributions in this .PSECT.
0000 388 ; End of ADAPTERS array *****
0000 389 ;***** End of ADAPTERS array *****
0000 390
0000 391 ;***** NUM_PAGES array *****
0000 392 .PSECT $SSINIT$DATA2
0000 393 NUM_PAGES: ; Build "number of pages to map" array.
0000 394 .PSECT $SSINIT$DATA3 ; User contributions in this .PSECT.
0000 395 ;***** End of NUM_PAGES array *****
0000 396
0000 397 ;***** INIT_ROUTINES array *****
0000 398 .PSECT $SSINIT$DATA4
0000 399 INIT_ROUTINES: ; Build "address of init routine" array.
0000 400 .PSECT $SSINIT$DATA5 ; User contributions in this .PSECT.
0000 401 ;***** End of INIT_ROUTINES array *****
0000 402
0000 403
0000 404 ; To add a new adapter type:
0000 405 ; 1) Add a new ADAPDESC macro invocation to the end of this list.
0000 406
0000 407 .PSECT $SSINIT$DATA,LONG
0000 408
0000 409
0000 410 ; Default interrupt vectors for UNIBUS system devices
0000 411 ; (This array is indexed by the RPB field RPBSB_DEVTYPE, if the RPB field
0000 412 ; RPBSW_ROUBVEC is zero. If RPBSW_ROUBVEC is not zero, then RPE:1 ROUBVEC
0000 413 ; is used and this array is not referenced at all. RPBSW_ROUBVEC is set up
0000 414 ; by PQDRIVER. RPBSL_BOOTRO is set by VMB to contain the device name in
0000 415 ; ASCII, not the vector number and device type, as it does on full
0000 416 ; architecture VAX machines.
0000 417
0000 418 BOOTVECTOR:
0088 419 .WORD ^X88 ; RK06/7 interrupt vector
0070 420 .WORD ^X70 ; RL01/2 interrupt vector
0004 421
0004 422 BUS_CSR_LEN:
00 423 .BYTE 0 ; Static byte containing the length (in bytes)
0005 424 ; of the adapter type field in the CSR's of
0005 425 ; the bus currently being configured. The
0005 426 ; proper value for the bus of interest is
0005 427 ; copied here, from the current nexus
0005 428 ; descriptor table, when we enter subroutine
0005 429 ; CONFIG_IOSPACE.
00000000 430 SW_BUS_CODE:
0005 431 .LONG 0 ; Static longword containing the software
0009 432 ; defined bus type, of the bus currently being
0009 433 ; configured, in the high order byte. The
0009 434 ; proper value for the bus of current interest
0009 435 ; is copied here, from the nexus descriptor

```

0009 436 ; CONFIG_IOSPACE.
0009 437
0009 438 DIRECT_VEC_NODE_CNT: ; Static longword that counts the number of
00000000 0009 439 ; direct vectoring adapter nodes that we have
00000000 0009 440 .LONG 0 ; run across so far.
00000001 000D 441
00000001 000D 442 \$SSVMSDEFINED = 1 ; Define symbol that means VMS system software.
00000080 000D 443 NUMUBAVEC = 128 ; ALLOW FOR 128 UNIBUS VECTORS
00000000 000D 444
00000000 000D 445 ADAPDESC - ; Memory. ** MUST BE 1ST IN DESCRIPTOR LIST **
00000000 000D 446 ADPTYPES=<NDTS_MEM1664NI,NDTS_MEM4NI,NDTS_MEM4I,NDTS_MEM16NI, -
00000000 000D 447 NDTS_MEM16I, -
00000000 000D 448 NDTS_MEM64NIL,NDTS_MEM64EIL,NDTS_MEM64NIU,NDTS_MEM64EIU, -
00000000 000D 449 NDTS_MEM64I, -
00000000 000D 450 NDTS_MEM256NIL,NDTS_MEM256EIL,NDTS_MEM256NIU,NDTS_MEM256EIU, -
00000000 000D 451 NDTS_MEM256I, -
00000000 000D 452 NDTS_SCORMEM> -
00000000 000D 453 NUMPAGES=1
00000000 000D 454
00000000 000D 455 ADAPDESC - ; MASSbus.
00000000 000D 456 ADPTYPES=NDTS_MB, -
00000000 000D 457 NUMPAGES=8, -
00000000 000D 458 INITRTN=INI\$MBADP
00000000 000D 459
00000000 000D 460 ADAPDESC - ; UNIBUS.
00000000 000D 461 ADPTYPES=<NDTS_UB0,NDTS_UB1,NDTS_UB2,NDTS_UB3,NDTS_BUA>, -
00000000 000D 462 NUMPAGES=8, -
00000000 000D 463 INITRTN=INI\$UBSPACE
00000000 000D 464
00000000 000D 465 ADAPDESC - ; Multi-port memory.
00000000 000D 466 ADPTYPES=<NDTS_MP0,NDTS_MP1,NDTS_MP2,NDTS_MP3>, -
00000000 000D 467 NUMPAGES=1, -
00000000 000D 468 INITRTN=INI\$MPMADP
00000000 000D 469
00000000 000D 470 ADAPDESC - ; DR32.
00000000 000D 471 ADPTYPES=NDTS_DR32, -
00000000 000D 472 NUMPAGES=4, -
00000000 000D 473 INITRTN=INI\$DRADP
00000000 000D 474
00000000 000D 475 ADAPDESC - ; C1780
00000000 000D 476 ADPTYPES=NDTS_C1, -
00000000 000D 477 NUMPAGES=9, -
00000000 000D 478 INITRTN=INI\$C1ADP
00000000 000D 479
00000000 000D 480 ADAPDESC - ; KDZ11 Processor
00000000 000D 481 ADPTYPES=NDTS_KDZ11, -
00000000 000D 482 NUMPAGES=1, -
00000000 000D 483 INITRTN=INI\$KDZ11
00000000 000D 484

```

000D 488 : TABLES OF ADAPTER-DEPENDENT INFORMATION
000D 489
000D 490
000D 491 : THE TABLE OFFSETS ARE:
000D 492
000D 493 : $DEFINI ADPTAB
000D 494
00000001 0000 495 ADPTAB_IDBUNITS:.BLKB 1 : # UNITS TO SET IN IDB
00000003 0001 496 ADPTAB_ADPLEN: .BLKW 1 : LENGTH OF ADP
00000004 0003 497 ADPTAB_ATYPE: .BLKB 1 : ADP TYPE
0004 498
0004 499 : $DEFEND ADPTAB
000D 500
000D 501 : TABLES THEMSELVES:
000D 502
000D 503
000D 504
000D 505 MBATAB: : TABLE OF MBA CONSTANTS
  UD 000D 506 .BYTE 8 : # UNITS IN MBA IDB
0030 000E 507 .WORD ADPSC_MBAADPLEN : # BYTES IN MBA ADP
  00 0010 508 .BYTE ATS_MBA : MBA ADAPTER TYPE
  01 0011 509
0011 510 DRTAB: : TABLE OF DR32 CONSTANTS
  0030 0011 511 .BYTE 1 : # UNITS IN DR IDB
  0030 0012 512 .WORD ADPSC_DRADPLEN : # BYTES IN DR ADP
  02 0014 513 .BYTE ATS_DR : DR ADAPTER TYPE
  0015 514
  0015 515 CITAB: : TABLE OF CI CONSTANTS
  0030 0015 516 .BYTE 1 : # UNITS IN CI IDB
  0030 0016 517 .WORD ADPSC_CIADPLEN : # BYTES IN CI ADP
  04 0018 518 .BYTE ATS_CI : CI ADAPTER TYPE
  0019 519

```

```

0019 523 .SBTTL CPU-specific data structures
0019 524
0019 525 : To add a new CPU type:
0019 526 : 1) Create a new nexus descriptor table, using FLOAT_NEXUS and
0019 527 : FIXED_NEXUS macros. Put an END_NEXUSDESC macro at the end.
0019 528 :
0019 529 :
0019 530 :
0019 531 :
0019 532 :
0019 533 :
0019 534 :
0019 535 CPU_APDSIZE:
0258 0019 536 .WORD ADPSC_UBAADPLEN
001B 537
001B 538
001B 539 :
001B 540 : Declare the beginning of a nexus-descriptor table.
001B 541 :
001B 542 : NEXUSDESC_TABLE LABEL=NEXUSDESC
0020 543
0020 544
0020 545 :
0020 546 : Describe all possible nexuses on an 11/750 (the first 10 have fixed adapter
0020 547 : assignments).
0020 548 :
00000000 0020 549 SBI_CPU = 0
00000000 0020 550 BI_CPU = 0
0020 551 : FIXED_NEXUS -
0020 552 : PHYSADR=I0750$AL_I0BASE, -
0020 553 : PERNEX=I0750$AL_PERNEX, -
0020 554 : NEXUSTYPES=<NDTS_MEM1664NI, -
0020 555 : NDTS_MPM0, -
0020 556 : NDTS_MPM1, -
0020 557 : NDTS_MPM2, -
0020 558 : NDTS_MB, -
0020 559 : NDTS_MB, -
0020 560 : NDTS_MB, -
0020 561 : NDTS_MB, -
0020 562 : NDTS_UB0, -
0020 563 : NDTS_UB1>
0020 564 :
0020 565 :
0020 566 :
0020 567 :
0020 568 :
0070 569
0070 570
0070 571
0070 572
0070 573
0070 574
0070 575
0070 576
0070 577
0070 578
0070 579
0070 580
0070 581
0070 582
0070 583
0070 584
0070 585
0070 586
0070 587
00A0 588
00A4 590
00A4 617
00A4 659
00A4 660
00A4 682
00A4 706
00A4 707
00A4 708 : Nexus "descriptor" arrays -- these arrays hold the nexus-device type and
00A4 709 : virtual address of every adapter on the system. The arrays, CONFREGL and
00A4 710 : SBICONF, are allocated enough space to hold the maximum number of adapters
00A4 711 : that can be attached to any CPU. When the code discovers how many adapters
00A4 712 : actually exist on the system, it will allocate space from non-paged pool
00A4 713 : and move a permanent copy of these arrays into that space.
00A4 714 :

```

00000040	00A4	715	MAXNEXUS = 64	
	00A4	716	CONFREG:	; Byte array of nexus-device type codes..
000000E4	00A4	717	.BLKB	MAXNEXUS
	00E4	718	SBICONF:	
000001E4	00E4	719	.BLKL	MAXNEXUS
	01E4	720	CONFREGL:	; Longword array of VAs of adapter space.
000002E4	01E4	721	.BLKL	MAXNEXUS

02E4 723 .SBTTL Message strings
0000000D 02E4 724
0000000A 02E4 725 CR = 13
02E4 726 LF = 10
02E4 727 NOSPT:
2D 54 49 4E 49 43 45 58 45 25 0A 0D 02E4 728 .ASCIZ <CR><LF>/%EXECINIT-F-Insufficient SPT entries/<CR><LF>
65 69 63 69 66 66 75 73 0F 49 2D 46 02F0
69 72 74 6E 65 20 54 50 53 20 74 6F 02FC
00 0A 0D 73 65 030B
030D
2D 54 49 4E 49 43 45 58 45 25 0A 0D 030D 730 BADUMR:
6D 65 6D 20 53 55 42 49 4E 55 2D 46 0319
74 6F 6E 20 73 65 6F 64 20 79 72 6F 0325
0D 30 20 74 61 20 74 72 61 74 73 20 0331
00 0A 033D

02E4 723 .SBTTL Message strings
02E4 724
02E4 725 CR = 13
02E4 726 LF = 10
02E4 727 NOSPT:
02E4 728 .ASCIZ <CR><LF>/%EXECINIT-F-Insufficient SPT entries/<CR><LF>
02E4 729 .ASCIZ <CR><LF>/%EXECINIT-F-UNIBUS memory does not start at 0/<CR><LF>
02E4 730 BADUMR:
02E4 731 .ASCIZ <CR><LF>/%EXECINIT-F-UNIBUS memory does not start at 0/<CR><LF>

033F 734 .SBTTL INISIOMAP, Initialize and map nexuses
 033F 735 +4
 033F 736 FUNCTIONAL DESCRIPTION:
 This routine is executed only once, during system initialization.
 It loops through all nexuses on the system, testing for
 adapters. When it finds an adapter, it maps its I/O space and
 initializes it.
 033F 737
 033F 738
 033F 739
 033F 740
 033F 741
 033F 742
 033F 743
 033F 744
 033F 745
 033F 746
 033F 747
 033F 748
 033F 749
 033F 750
 033F 751
 033F 752
 033F 753
 033F 754
 033F 755
 033F 756
 033F 757
 033F 758
 033F 759
 033F 760
 033F 761
 033F 762
 033F 763
 033F 764
 033F 765
 033F 766
 033F 767
 033F 768
 033F 769
 033F 770
 033F 771
 033F 772 --
 033F 773
 033F 774 .PSECT SSSINIT\$CODE,QUAD
 033F 775 INISIOMAP:::
 0FFF 8F 88 0000 776
 0FFF 8F 88 0000 777
 0FFF 8F 88 0004 778
 0FFF 8F 88 0004 779
 0FFF 8F 88 0004 780
 Set up common inputs to CONFIG_IOSPACE subroutine for the CPU-specific code.
 52 00000000'GF D0 0004 781
 53 00000000'GF D0 0008 782
 53 6342 DE 0012 783
 52 52 09 78 0016 784
 52 80000000 8F C8 001A 785
 54 D4 0021 786
 59 00000000'GF D0 0023 787
 5A 5C A9 F7 8F 78 002A 788
 00000000'GF 00E4'CF DE 0030 791
 00000000'GF 00A4'CF DE 0039 792
 00000000'GF 01E4'CF DE 0042 793
 MOVL G^BOOSGL_SPTFREL,R2 ; Get next available VPN.
 MOVL G^MMG\$GL_SPTBASE,R3 ; Get base of System Page Table.
 MOVAL (R3)[R2],R3 ; Compute SVASPT.
 ASHL #9,R2,R2 ; Convert VPN to VA.
 BISL #VASM_SYSTEM,R2 ; Set system bit.
 CLRL R4 ; Clear index into CONFREG and SBICONF.
 MOVL G^EXESGL_RPB,R9 ; Get address of RPB.
 ASHL #9,RPBSL_ADPPHY(R9),R10 ; Get PFN of boot adapter space.
 MOVAL W^SBICONF,G^MMG\$GL_SBICONF ; Set pointers to local copies
 MOVAL W^CONFREG,G^EXESGL_CONFREG ; of these arrays for init routines.
 MOVAL W^CONFREGL,G^EXESGL_CONFREGL ; ...

004B 899 .SBTTL INITADP_780, _750, _730, and _UV1
004B 900 :
004B 901 : I/O address space for the 11/780, 11/750, 11/730, and Micro-VAX I cpus
004B 902 : is statically defined in their respective nexus descriptor tables.
004B 903 :
56 0020'CF DE 004B 904 MOVAL W^NEXUSDESC,R6 : Get address of nexus table.
5B D4 0050 905 CLRL R11 : Signal use 1st page of SCB.
0B 10 0052 906 BSBB CONFIG_IOSPACE : Configure processor I/O space.
0054 907
0054 909
00C3 30 0054 910 BSBW CREATE_ARRAYS : Create CONFREG and SBICONF arrays.
0FFF 8F BA 0057 911 POPR #^M<R0,R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11>
50 01 D0 005B 912 MOVL #1,R0 : Set success status
05 005E 913 RSB : Return.

005F 916 .SBTTL CONFIG_IOSPACE
 005F 917
 005F 918 CONFIG_IOSPACE
 005F 919 Given a nexus descriptor table, which describes what "nexuses" or
 005F 920 "slots" are available on a system to hold I/O adapters, find and
 005F 921 initialize all adapters on the system.
 005F 922
 005F 923 Inputs:
 005F 924 R2 - next available virtual address, to be used for mapping I/O space
 005F 925 R3 - address of PTE associated with VA in R2
 005F 926 R4 - Current index into CONFREG and SBICONF arrays (should be 0 the
 005F 927 first time CONFIG_IOSPACE is called)
 005F 928 R6 - address of nexus descriptor table
 005F 929 R9 - address of Restart Parameter Block (RPB)
 005F 930 R10 - PFN of boot adapter space
 005F 931 R11 - page offset from beginning of SCB; tells which page of the SCB
 005F 932 to use for this set of nexuses (passed to routines that init ADP)
 005F 933
 005F 934 Outputs:
 005F 935 R2, R3, R4 - updated
 005F 936 R9, R10, R11 - preserved; all other registers potentially modified
 005F 937 CONFREG - initialized with adapter NDT\$ code for each nexus
 005F 938 SBICONF - initialized with adapter space VA for each nexus
 005F 939
 005F 940 CONFIG_IOSPACE:
 005F 941
 005F 942 Main loop. Map and initialize all adapters on system.
 005F 943
 005F 944
 005F 950
 FB A6 90 005F 951 MOVB CSR_LEN_OFFSET(R6),- ; Move length of adapter type field
 0004'CF 0062 952 W^B0\$ CSR_LEN ; in CSR's to static location.
 FC A6 D0 0065 953 MOVL BUS_CODE_OFFSET(R6),- ; Move software defined bus type code
 0005'CF 0068 954 W^SQ_BUS_CODE ; to static longword.
 006B 955
 006B 956 NXT_NEXUS:
 58 86 D0 006B 957 MOVL (R6)+,R8 ; For each nexus...
 01 12 006E 958 BNEQ TEST_NEXUS ; Get PFN of nexus.
 05 0070 959 RSB ; If PFN non-zero, go test the slot.
 0071 960 ; If 0, we've found all nexuses.
 0071 961
 0071 962 ; Read configuration register to determine if anything is present at this
 0071 963 ; nexus.
 0071 964
 0071 965 TEST_NEXUS:
 90000000 8F C9 0071 966 BISL3 #PTE\$M VALID!PTE\$C_KW,- ; Temporarily associate VA in R2 with
 63 58 0077 967 R8, (R3) ; PFN in R8 via SPTE in R3.
 0079 968 SPRCTCTINI B^10\$, - ; Protect following code from non-
 51 62 D0 0085 969 #<MCHK\$M_NEXM!MCHK\$M_LOG>; existent memory machine checks.
 0088 970 MOVL (R2), R1 ; Read adapter configuration register.
 0089 971 SPRCTCTEND 10\$; End of protected code.
 11 50 E8 008C 972 INVALID R2 ; Clear TB of temporary mapping.
 008F 973 BLBS R0, GET_TYPE ; Branch if no machine check occurred.
 008F 974
 008F 975 ; No adapter present at this nexus.
 008F 976
 00A4'CF44 94 008F 977 CLRB W^CONFREG[R4] ; Store "unknown" type in CONFREG
 01E4'CF44 D4 0094 978 CLRL W^CONFREGL[R4] ; and in CONFREGL also.
 55 D4 0099 979 CLRL R5 ; Use general memory type to map

56 04 C0 009B 980 : one page of I/O space.
59 11 009B 981 ADDL2 #4, R6
009E 982 BRB MAP_NEXUS : Step past type code in nexus table.
00A0 984 : Go map I/O space for this nexus.
00A0 985 : Execution continues here if adapter was present.
00A0 986 :
57 86 D0 00A0 987 GET_TYPE:
14 12 00A0 988 MOVL (R6)+, R7 : Get nexus-device type from nexus table.
00A2 989 BNEQ GET_GEN_TYPE : Branch if fixed slot.
00A2 990 :
00A2 991 : Floating-type slot. Use type from configuration register.
00A2 992 : Determine if type in configuration register is 8-bits or 16-bits.
00A2 993 :
00A2 994 :
0004'CF 01 91 00A5 995 :
00A5 996 CMPB #1, W^BUS_CSR_LEN : Determine length of adapter type
00AA 997 field in CSR contained in R7.
57 05 13 00AA 998 BEQL 10\$: EQL implies 1 byte (8-bit) field.
51 3C 00AC 999 MOVZWL R1, R7 : BI_LIKE, so use word instruction.
03 11 00AF 1000 BRB 20\$: Skip byte instruction.
57 51 9A 00B1 1001 10\$: MOVZBL R1, R7 : Use byte instruction to get type.
57 0005'CF C8 00B4 1002 20\$: BISL W^SW_BUS_CODE, R7 : Or in software bus code.
00B4 1003 :
00B9 1004 : Here R7 has hardware adapter code or'ed with software bus code.
00B9 1005 :
00B9 1006 : Translate specific nexus device type code into general adapter type code.
00B9 1007 :
00B9 1008 :
00B9 1009 GET_GEN_TYPE:
00A4'CF44 57 90 00B9 1010 MOVB R7, W^CONFREG[R4] : Save nexus-device type in CONFREG.
01E4'CF44 57 D0 00BF 1011 MOVL R7, W^CONFREGL[R4] : CONFREGL also filled in.
55 D4 00C5 1012 CLRL R5 : Clear loop index.
50 0000'CF45 DE 00C7 1013 30\$: MOVAL W^ADAPTERS[R5], R0 : Get address of adapter type code.
0000'CF 9F 00CD 1014 PUSHAB W^NUM_PAGES : Push addr of end of ADAPTERS array.
8E 50 D1 00D1 1015 CMPL R0, (SP)+ : See if we went beyond array.
3F 1E 00D4 1016 BGEOU END_NEXUS : unrecognized adapter, do not map.
60 57 D1 00D6 1017 CMPL R7, (R0) : Adapter type match?
04 13 00D9 1018 BEQL 40\$: If EQL yes, adapter type match.
55 D6 00DB 1019 INCL R5 : Increment loop index.
E8 11 00DD 1020 BRB 30\$: Look at next adapter.
00DF 1021 :
00DF 1022 40\$: :
00DF 1023 :
00DF 1024 : Store boot parameters.
00DF 1025 :
00DF 1026 :
5A 58 D1 00DF 1028 CMPL R8, R10 : Does PFN match boot adapter's PFN?
15 12 00E2 1029 BNEQ MAP_NEXUS : No; continue.
60 A9 52 D0 00E4 1031 MOVL R2, RPB\$L_ADPVIR(R9) : Store VA of boot adapter space.
20 A9 54 D0 00E8 1032 MOVL R4, RPB\$L_BOOTR1(R9) : Store boot adapter nexus number.
51 54 A9 0D 00 EF 00EC 1033 EXTZV #0, #15, = : Get offset into UNIBUS/QBUS I/O page.
58 A9 1000 C241 9E 00F2 1034 MOVAB <8*512>(R2)[R1], - : Set VA of UNIBUS/QBUS registers.
00F2 1035 RPB\$L_CSRPHY(R9), R1
00F9 1036 RPB\$L_CSRVIR(R9)
00F9 1037 :
00F9 1038 :
00F9 1039 : R5/ general adapter type; index into "general" adapter arrays.
00F9 1040 : For each adapter -

00E4'CF44 52 DD 00F9 1042 : Map the # of pages specified in ADAPDESC macro
51 0000'CF45 3C 00FF 1043 : JSB to initialization routine specified in ADAPDESC macro
51 0000'CF45 6C 10 0105 1044 :
61 0107 1052 :
04 13 010F 1055 :
00 B141 16 0111 1056 :
FF51 54 D6 0115 1057 :
31 0117 1060 :
011A 1064 :
00F9 1045 : MAP_NEXUS:
MOVW R2,W\$SBICONF[R4]
MOVZWL W\$NUM_PAGES[R5],R1
BSBB MAP_PAGES
MOVAL W\$INIT_ROUTINES[R5],R1
TSTL (R1)
BEQL END_NEXUS
JSB A(RT)[R1]
END_NEXUS:
INCL R4
BRW NXT_NEXUS
: Save VA of adapter space in SBICONF.
: Get number of pages to map.
: Map the I/O pages.
: Get address of initialization routine.
: Initialization routine specified?
: Branch if none.
: Call initialization routine.
: Increment CONFREG and SBICONF index.
: Go do next nexus.

011A	1066	.SBTTL CREATE_ARRAYS			
011A	1067	CREATE_ARRAYS			
011A	1068	Move the local CONFREG and SBICONF arrays into non-paged pool.			
011A	1069	Inputs:			
011A	1070	R4 - Number of nexuses on the system.			
011A	1071	CONFREG and SBICONF have been initialized.			
011A	1072	Outputs:			
011A	1073	R0 - R5 destroyed			
011A	1074	EXESGL_CONFREG points to a copy of the CONFREG array in non-paged pool			
011A	1075	MMGSGL_SBICONF points to a copy of the SBICONF array in non-paged pool			
011A	1076	EXESGL_NUMNEXUS contains the number of nexuses on the system			
00000000'GF	54	00	011A	1083	CREATE_ARRAYS:
51	0C A444	DE	0121	1084	MOVL R4,G^EXESGL_NUMNEXUS ; Store number of nexuses on system.
		DE	0126	1085	MOVAL 12(R4)[R4],R1 ; Allocate n bytes for CONFREG plus
51	6144	DE	0126	1086	4n bytes for SBICONF + header
	01F9	30	012A	1087	MOVAL (R1)[R4],R1 ; Another 4n bytes for CONFREGL.
	82	7C	012D	1088	BSBW ALONPAGD ; Get pool for CONFREG and SBICONF.
82	51	80	012F	1089	CLRQ (R2)+ ; Clear out unused
00000000'GF	0763	8F	80	0132	MOVW R1,(R2)+ ; Set in size
51	6244	9E	0137	1090	MOVW #<DYNSC_CONF8>!DYNSC_INIT,(R2)+ ; Set type and sub-type
00000000'GF	6244	9E	013E	1091	MOVAB (R2) G^EXESGL_CONFREG ; Store address of system CONFREG.
00000000'GF	51	DO	0142	1092	MOVAB (R2)[R4],R1 ; Two steps to CONFREGL, 1st, SBICONF.
00000000'GF	6144	DE	0149	1093	MOVL R1,G^MMGSGL_SBICONF ; Store address of system SBICONF.
	14	BB	0151	1094	MOVAL (R1)[R4],G^EXESGL_CONFREGL ; And address of system CONFREGL.
62	00A4'CF	54	28	0153	PUSHR #^M<R2,R4> ; Save pool address and nexus count.
	14	BA	0159	1095	MOVC3 R4,W^CONFREG,(R2) ; Copy CONFREG to pool.
51	54	04	C5	015B	POPR #^M<R2,R4> ; Retrieve pool address and nexus count.
6244	00E4'CF	51	28	0162	MULL3 #4,R4,R1 ; Number of bytes in SBICONF.
	7E	51	DO	0169	MOVL R1,-(SP) ; Save, SBICONF size = CONFREGL size
	51	8E	DO	016C	MOVC3 R1,W^SBICONF,(R2)[R4] ; Copy SBICONF to pool.
63	01E4'CF	51	28	0172	MOVL (SP)+,R1 ; Restore size of SBICONF and CONFREGL.
	0172	1104	MOVC3 R1,W^CONFREGL,(R3) ; Copy CONFREGL to pool. R3 is output		
	0172	1105		from SBICONF MOVC3, so SBICONF and	
	0172	1106		CONFREGL must be adjacent.	
05	0172	1107	RSB		

0173 1109 .SBTTL MAP_PAGES
 0174 1110 ++
 0174 1111 : INPUTS:
 0174 1112 R1/ Number of pages to map.
 0174 1113 R2/ VA of page to map.
 0174 1114 R3/ VA of system page table entry to be used.
 0174 1115 R8/ PFN of page(s) to map.
 0174 1116
 0174 1117 : OUTPUTS:
 0174 1118 R2,R3 updated; R1,R8 destroyed; all other registers preserved
 0174 1119
 0174 1120 :--
 0174 1121
 0174 1122 MAP_PAGES:
 0174 1123
 83 58 90000000 BF C9 0173 1124 BISL3 #<PTESM_VALID!PTESC_KW>,R8,(R3)+
 52 58 0200 C2 D6 0178 1125 : Map a page.
 00000000'GF 00000000'GF 9E 017D 1126 INCL R8 : Next PFN.
 00000000'GF 00000000'GF D6 0182 1127 MOVAB 512(R2),R2 : Next VA.
 06 DB 51 D1 0188 1128 INCL G^BOO\$GL_SPTFREL : Next free entry.
 04 F5 0193 1129 CMPL G^BOO\$GL_SPTFREH, - : Check for no more system page
 05 0198 1130 G^BOO\$GL_SPTFREL : table entries.
 0199 1131 BLEQ ERROR_HALT : Branch if out of SPTEs.
 0199 1132 SOBGTR R1,MAP_PAGES : Map another page.
 0199 1133 RSB : All done.
 51 02E4'CF 9E 0199 1135 ERROR_HALT:
 00000000'GF 00000000'GF 019E 1136 MOVAB W^NOSPT,R1 : Set error message.
 019E 1137 ERROR_HALT 1: CLRL R11 : Indicate console terminal.
 00 01A0 1138 JSB G^EXESOUTZSTRING : Output error message.
 00 01A6 1140 HALT : ***** FATAL ERROR *****

01A7	1269	.SBTTL INI\$UBSPACE			
01A7	1270	::: Map UNIBUS space; initialize UNIBUS ADP.			
01A7	1271	INPUTS:			
01A7	1272	R2 - VA of next free system page			
01A7	1273	R3 - VA of system page table entry to be used to map VA in R2			
01A7	1274	R4 - nexus identification number of this adapter			
01A7	1275	-8(R6) - PFN of this UNIBUS adapter's register space			
01A7	1276				
01A7	1277				
01A7	1278				
01A7	1279	OUTPUTS:			
01A7	1280	UNIBUS space is mapped.			
01A7	1281	INI\$UBADP is called to build an ADP block and initialize UNIBUS			
01A7	1282	adapter hardware.			
01A7	1283	:::			
01A7	1284	::--			
01A7	1285				
01A7	1286	INI\$UBSPACE:			
01A7	1287				
58 58 01E4'CF44 DE	01A7 1290	MOVAL	W^CONFREGL[R4],R8	; R8 => CONFREGL slot.	
68 02 00 EF	01AD 1291	EXTZV	#0,#2,(R8),R8	; Get UBA number.	
58 58 09 78	01B2 1292	ASHL	#9,R8,R8	; Position UB number.	
	01B6 1295				
	01B6 1304				
	01B6 1309				
58 00007FF0 BF 58 C3	01B6 1311	SUBL3	R8,#<I0750\$AL_UB0SP+^0760000/^X200>,R8	; Get PFN of UB I/O page.	
	01BE 1312				
	01BE 1314				
	01BE 1319				
	01BE 1325				
	01BE 1330				
51 10 DD FFAF 30	01BE 1331	MOVL	#16,R1	; Number of pages to map (UB/Qbus space).	
	01C1 1332	BSBW	MAP_PAGES	; Map I/O pages.	
	01C4 1333	:: Call adapter initialization routine.			
	01C4 1334				
	01C4 1335				
	01C4 1336	BSBW	INI\$UBADP	; Init ADP block.	
	01C4 1337		RSB		

01C4 1339 .SBTTL INISUBADP - BUILD ADP AND INITIALIZE UBA
 01C4 1340 :+
 01C4 1341 :+ INISUBADP ALLOCATES AND FILLS IN AN ADAPTER CONTROL BLOCK, INTERRUPT
 01C4 1342 :+ DISPATCHER AND CONNECTS THEM TO THE PROPER SCB VECTORS. A CALL IS
 01C4 1343 :+ THEN MADE TO UBAINITIAL TO INITIALIZE THE ADAPTER HARDWARE.
 01C4 1344 :+
 01C4 1345 :+ INPUT:
 01C4 1346 :+ R4 - nexus identification number of this adapter
 01C4 1347 :+ R11- offset from beginning of SCB to correct SCB page for this adapter
 01C4 1348 :+
 01C4 1349 :+
 01C4 1350 INISUBADP:
 01FF 8F BB 01C4 1351 PUSHR #^M<R0,R1,R2,R3,R4,R5,R6,R7,R8> ; SAVE R0-R8
 01C4 1352 :+
 01C8 1353 :+ Allocate and initialize Adapter Control Block (ADP).
 01C8 1354 :+
 01C8 1355 :+
 S1 0019'CF 3C 01C8 1356 MOVZWL W^CPU ADPSIZE,R1 : PICK UP LENGTH OF ADP
 0156 30 01CD 1357 BSBW ALONPAGD : ALLOCATE SPACE FOR ADP
 08 A2 51 B0 01D0 1358 MOVW R1,ADPSW_SIZE(R2) : SET SIZE INTO ADP BLOCK
 0A A2 01 90 01D4 1359 MOVB #DYNSC ADP, - : AND SET TYPE OF BLOCK
 0E A2 01 B0 01D8 1360 MOVB ADPSB_TYPE(R2)
 62 00E4'CF44 D0 01DC 1361 MOVW #ATS UBA, - : SET TYPE OF ADAPTER
 0C A2 54 B0 01E2 1362 MOVL W^SBI[CONF[R4], - : SET VA OF CONFIGURATION REG
 04 A0 50 B0 01E2 1363 MOVL ADPSL_CSR(R2)
 50 14 A2 DE 01E6 1364 MOVW R4,ADPSW_TR(R2) : SET TR NUMBER FOR ADAPTER
 60 50 D0 01EA 1365 MOVAL ADPSL_DPOFL(R2),R0 : ADDRESS OF DATA PATH WAIT QUEUE
 04 A0 50 D0 01ED 1366 MOVL R0,(R0) : INIT QUEUE HEADER
 MOVL R0,4(R0)
 50 30 A2 DE 01F1 1367 MOVAL ADPSL_MRQFL(R2),R0 : ADDRESS OF MAP WAIT QUEUE
 60 50 D0 01F5 1371 MOVL R0,(R0) : INIT QUEUE HEADER
 04 A0 50 D0 01F8 1372 MOVL R0,4(R0)
 04 A2 D4 01FC 1373 CLRL ADPSL_LINK(R2) : ZAP ADAPTER CHAIN LINK
 FDFE 30 01FF 1374 BSBW ADPLINK : LINK ADP TO END OF LIST
 58 00000000'GF D0 0202 1375 :+ Initialize adapter interrupt vectors in System Control Block.
 0202 1376 :+
 0202 1377 :+
 0202 1378 :+
 0202 1379 :+ MOVL G^EXESGL_SCB,R8 : GET SCB ADDRESS
 0209 1380 :+
 0209 1381 :+
 0209 1447 :+
 0209 1449 :+
 0209 1450 :+
 0200 28 DD 0209 1451 PUSHL #NDTS_UB0
 0200 C8 DE 0208 1451 MOVAL ^X200(R8), - : ASSUME UBO
 10 A2 020F 1452 ADPSL_VECFOR(R2) : GET VECTOR SPACE FOR UBO
 28 01E4'CF44 D1 0211 1453 CMPL W^CONFREG[R4],#NDTS_UB0 : IS DEVICE TYPE = UBO?
 08 13 0217 1454 BEQL 10\$: BRANCH IF SO
 10 A2 00000200 8F C0 021C 1455 MOVL #NDTS_UB1,(SP) : INDICATE UB1
 60 A2 0E B0 0224 1456 ADDL #^X200,ADPSL_VECTOR(R2) : STEP TO ITS VECTOR SPACE
 53 62 D0 0228 1457 10\$: MOVL #^XE,ADPSW_DPBITMAP(R2) : MARK DATAPATHS 1-3 AVAILABLE
 53 0800 C3 9E 0228 1458 MOVL ADPSL_CSR(R2),R3 : VIRTUAL ADDRESS OF ADAPTER
 54 01F0 8F 3C 0230 1459 MOVAB UBA\$L_MAP(R3),R3 : POINT TO MAPPING REGISTERS
 83 D4 0235 1460 MOVZWL #496,R4 : NUMBER OF UMR TO DISABLE
 1461 20\$: CLRL (R3)+ : DISABLE A UNIBUS MAP REGISTER

53 00000001'GF FB 54 F5 0237 1462 SO9GTR R4,20\$: LOOP THRU THEM ALL
 DE 023A 1463 MOVAL G^UBASUNEXINT+1,R3 : GET ADDR OF UNEXP INT SERVICE
 54 0001'CF DE 0241 1464 (+1 MEANS HANDLE ON INT STACK)
 0241 1465 MOVAL W^UBASINT0+1,R4 : SPECIAL CASE TO COUNT PASSIVE RELEASE
 0246 1466
 0246 1467 : INIT UB VECTORS TO UNEXPECTED INTERRUPT SERVICE
 0246 1468 :
 50 10 A2 D0 0246 1470 MOVL ADPSL_VECTOR(R2),R0 : GET ADDRESS OF VECTORS
 51 80 54 D0 024A 1471 MOVL R4,(R0)+ : SPECIAL CASE FOR VECTOR 0
 51 7F 8F 9A 024D 1472 MOVZBL #<NUMUBAVEC-1>,R1 : REST OF VECTORS
 80 53 D0 0251 1473 30\$: MOVL R3,(R0)+ : FILL VECTOR WITH UNEXP INT
 FA 51 F5 0254 1474 SOBGTR R1,30\$: FILL ALL VECTORS
 6E 29 91 0257 1475 CMPB #NDTS_UB1,(SP) : IS THIS UB1?
 3C 12 025A 1476 BNEQ 40\$: IF NOT, SKIP CODE
 025C 1477 :
 025C 1478 : SAVE CONTENTS OF SPTE'S MAPPING UB SPACE
 025C 1479 :
 54 52 D0 025C 1480 MOVL R2,R4 : SAVE ADP ADDRESS
 52 62 D0 025F 1481 MOVL ADPSL_CSR(R2),R2 : GET VA OF ADAPTER
 00000000'GF 16 0262 1482 JSB G^MMG\$SVAPTECHK : GET ADDRESS OF SPTE MAPPING ADAPTER
 54 A4 63 D0 0268 1483 MOVL (R3),ADPSL_UBASPTE(R4) : STORE CONTENTS OF SPTE IN ADP
 58 A4 20 A3 D0 026C 1484 MOVL <8*4>(R3),ADPSL_UBASPTE+4(R4) ; SAME FOR I/O SPACE
 0271 1485 :
 0271 1486 : CALCULATE AND STORE VA OF IPEC REGISTER, WHICH CONTAINS BITS NEEDED
 0271 1487 : TO PROCESS POWERFAIL
 00002464 8F C1 0271 1488 : ADDL3 #<8*^X200> + UASSW_IP_CR1.- : VA OF ADAPTER + OFFSET TO
 50 A4 52 0277 1490 R2,ADPSL_UBASCB+12(R4) ; I/O SPACE + OFFSET TO IPEC REGISTER
 027A 1491 :
 027A 1492 : STORE INTERRUPT CODE IN ADP, STORE ITS ADDRESS IN POWERFAIL INTERRUPT
 027A 1493 : VECTOR IN SCB, AND SAVE ITS ADDRESS IN ADP
 027A 1494 :
 48 A4 031E'CF 7D 027A 1495 MOVQ W^UBA1INT,ADPSL_UBASCB+4(R4)
 4A A4 0000'CF 9E 0280 1496 MOVAB W^EXESUBAERR_INT,ADPSL_UBASCB+6(R4)
 01E4 C8 48 A4 DE 0286 1497 MOVAL ADPSL_UBASCB+4(R4),^X1E4(R8)
 01E4 C8 D6 028C 1498 INCL ^X1E4(R8) : USE INTERRUPT STACK
 44 A4 48 A4 DE 0290 1499 MOVAL ADPSL_UBASCB+4(R4),ADPSL_UBASCB(R4)
 0295 1500 :
 0295 1501 : DONE WITH ADAPTER-SPECIFIC CODE
 52 54 D0 0295 1502 :
 5E 04 C0 0298 1503 MOVL R4,R2 : RESTORE R2
 0298 1504 40\$: ADDL #4,SP : CLEAN STACK
 0298 1505 :
 0298 1506 :
 0298 1507 :
 0298 1508 :
 0298 1536 :
 0298 1537 :
 0298 1558 :
 0298 1559 :
 0298 1601 :
 0298 1602 :
 0298 1651 :
 0298 1652 : Now check for any UNIBUS memory that may be on the adapter. First we must
 0298 1653 : disable all the UNIBUS Map Registers so that there is no conflict in
 0298 1654 : which memory will respond. Then we check all 248Kb of potential memory in
 0298 1655 : 8Kb chunks, since each disable bit on the 780 UBA represents 16 UMR's or

029B 1656 : 8Kb of memory. The number of registers is stored in the ADP and the
029B 1657 : corresponding number withdrawn from the UMR map in the ADP.
029B 1658 :
029B 1659 :
56 62 D0 029B 1661 MOVL ADPSL_CSR(R2),R6 : Pick up adapter pointer
51 D4 029E 1662 CLRL R1 : Zero out number of UMR to disable
08 AE 00000200 8F C3 02A0 1664 SUBL3 #512, 8(SP), R7 : R7 = VA of last page of UNIBUS
58 OC AE 04 C3 02A9 1665 SUBL3 #4, 12(SP), R8 : R8 = VA of SPTE mapping (R7)
54 20 AE 00000200 8F C3 02AE 1666 SUBL3 #512, 32(SP), R4 : R4 = PFN of first page of UNIBUS
68 DD 02B7 1667 PUSHL (R8) : Save contents of SPTE
53 54 D0 02B9 1668 MOVL R4, R3 : Copy starting PFN
55 1F D0 02BC 1669 MOVL #31, R5 : 31 8Kb chunks to test
90000000 8F C9 02C2 1670 50\$: INVALID R7 : Invalidate TB
68 54 02C8 1671 BISL3 #<PTESM_VALID!PTESC_KW>,- : Map each page of UNIBUS
50 57 D0 02CA 1672 MOVL R7, R0 : Address to check
FD 30 30 02CD 1673 BSBW EXTEST_CSR : Validate it
0D 50 E9 02D0 1674 BLBC R0, 70\$: Not there
54 53 D1 02D3 1675 CMPL R3, R4 : First time in?
04 13 02D6 1676 BEQL 60\$: Yes, skip next test
51 3A 13 02DA 1677 TSTL R1 : Any registers already?
54 10 A1 9E 02DC 1680 60\$: MOVAB 16(R1), R1 : No, memory not start at 0
54 10 A4 9E 02E0 1681 70\$: MOVAB 16(R4), R4 : Yes, up the count
D8 55 F5 02E4 1682 SOBGTR R5, 50\$: Map Next 8Kb (16*512)
68 8E D0 02E7 1683 POPL (R8) : Loop until done
0256 C2 51 80 02EA 1684 INVALID R7 : Restore old contents of SPTE
02ED 1686 MOVW R1, ADPSW_UMR_DIS(R2) : Invalidate TB
02F2 1688 : Record number disabled
02F2 1689 : Initialize fields for new UBA map register allocation. Make it appear
02F2 1690 : that we have one contiguous array of 496 available map registers.
02F2 1691 : To do this we set ADPSL_MRACTMDRS to one (the number of active
02F2 1692 : map register descriptors for distinct contiguous areas),
02F2 1693 : ADPSW_MRNRREGARY(0) to 496 (i.e. the number of registers in this
02F2 1694 : contiguous range) and ADPSFREGARY(0) to 0 (i.e. the first register
02F2 1695 : in the range is register 0).
02F2 1696 :
64 A2 5C A2 01 D0 02F2 1697 MOVL #1, ADPSL_MRACTMDRS(R2) : 1 active map descriptor
01F0 8F 51 A3 02F6 1698 SUBW3 R1, #496, ADPSW_MRNRREGARY(R2) : for a range of 496 registers
015E C2 51 B0 02FD 1710 MOVW R1, ADPSW_MRFREGARY(R2) : starting at register zero.
62 A2 01 AE 0302 1711 MNEGW #1, ADPSW_MRNFENCE(R2) : Also init "fences" which precede
015C C2 01 AE 0306 1712 MNEGW #1, ADPSW_MRFFENCE(R2) : the two descriptor arrays.
0308 1713 : Initialize adapter hardware.
0308 1714 :
54 62 FCEF 30 0308 1716 MOVL ADPSL_CSR(R2), R6 : Get CSR address to init
01FF BF BA 0311 1717 BSBW UBASINITIAL : And initialize adapter
05 0315 1718 POPR #^M<R0, R1, R2, R3, R4, R5, R6, R7, R8> : Restore registers
0316 1719 RSB : Return
0316 1720 :
0316 1721 : Error if UNIBUS memory not start at location 0
0316 1722 :
51 030D'CF FE80 9E 0316 1725 80\$: MOVAB W^BADUMR, R1 : Set error message
31 0318 1726 BRW ERROR_HALT_1 : Put it out
031E 1728 :

031E 1802 :
031E 1803 : UBA INTERRUPT SERVICE HANDLER FOR 11/750. THIS CODE IS PLACED
031E 1804 : IN THE ADP AND IT IS POINTED TO BY THE SCB VECTOR WHICH
031E 1805 : HANDLES UBA POWERFAIL INTERRUPTS. USING A JSB TO DISPATCH
031E 1806 : TO THE ADAPTER POWERFAIL INTERRUPT CODE ALLOWS A POINTER WITH A
031E 1807 : KNOWN OFFSET INTO THE ADP TO BE PUSHED ON THE STACK AND USED
031E 1808 : BY THE CODE TO FIND THE ADP.
031E 1809 :
031E 1810 : UBA1INT:

00000000 9F 16 031E 1811 JSB 2#0
0000 0324 1812 .WORD 0 ; ERROR ROUTINE IN ADPERR750
; ZERO OUT REST OF QUADWORD

0326 1815 .SBTTL INISMBADP - BUILD ADP AND INITIALIZE MBA
 0326 1816 .SBTTL INISDRADP - BUILD ADP AND INITIALIZE DR32
 0326 1817 .SBTTL INISCIADP - BUILD ADP AND INITIALIZE CI
 0326 1818 :+ INISMBADP IS CALLED AFTER MAPPING THE REGISTERS FOR A MASSBUS ADAPTER.
 0326 1819 : AN ADAPTER CONTROL BLOCK IS ALLOCATED AND FILLED. A CRB AND IDB ARE
 0326 1820 : ALSO ALLOCATED AND INITIALIZED. THE ADAPTER HARDWARE IS THEN INITIALIZED
 0326 1821 : BY CALLING MBASINITIAL.
 0326 1822 :+ INISDRADP IS CALLED AFTER MAPPING THE REGISTERS FOR THE DR32
 0326 1823 : ADAPTER. THE ADAPTER CONTROL BLOCK, CRB, AND IDB ARE ALLOCATED
 0326 1824 : AND INITIALIZED. THE ADAPTER HARDWARE IS THEN INITIALIZED BY
 0326 1825 : CALLING DRSSINITIAL.
 0326 1826 :+ INISMBADP AND INISDRADP SHARE COMMON CODE AFTER THE TABLE OF ADAPTER
 0326 1827 : SPECIFIC CONSTANTS IS SELECTED AND STORED IN R8.
 0326 1828 :
 0326 1829 :
 0326 1830 :
 0326 1831 :
 0326 1832 :
 0326 1833 :
 0326 1834 :
 0326 1835 :
 0326 1836 :
 0326 1837 :
 0326 1838 :
 0326 1839 :
 00000000'GF 17 0326 1840 ALONPAGD:JMP G^INISALONONPAGED
 032C 1841 .ENABL LSB
 032C 1842 :+ INISDRADP: : INITIALIZE DR32 DATA STRUCTURES
 032C 1843
 032C 1844
 032C 1845
 58 07FF 8F BB 032C 1846 PUSHR #^M<R0,R1,R2,R3,R4,R5,R6,R7,R8,R9,R10> : SAVE REGISTERS
 58 0011'CF DE 0330 1847 MOVAL W^DRTAB,R8 : GET DR32 TABLE OF CONSTANTS
 59 0000'CF 9E 0335 1848 MOVAB W^DRSINT,R9 : ADDRESS OF INTERRUPT SERVICE ROUTINE
 5A 0000'CF 9E 033A 1849 MOVAB W^DRSINITIAL,R10 : ADDRESS OF DEVICE INITIALIZATION
 28 11 033F 1850 BRB 10\$: JOIN COMMON CODE
 0341 1851 :+ INISCIADP: : INITIALIZE CI DATA STRUCTURES
 0341 1852
 0341 1853
 0341 1854
 0341 1855
 0341 1856
 0341 1857
 58 07FF 8F BB 0341 1858 PUSHR #^M<R0,R1,R2,R3,R4,R5,R6,R7,R8,R9,R10> : SAVE REGISTERS
 58 0015'CF DE 0345 1859 MOVAL W^CITAB,R8 : GET CI TABLE OF CONSTANTS
 59 0000'CF 9E 034A 1860 MOVAB W^CISINT,R9 : ADDRESS OF INTERRUPT SERVICE ROUTINE
 5A 0000'CF 9E 034F 1861 MOVAB W^CISINITIAL,R10 : ADDRESS OF DEVICE INITIALIZATION
 13 11 0354 1862 BRB 10\$: JOIN COMMON CODE
 0356 1863 :+ INISMBADP: : INIT MBA DATA STRUCTURES
 0356 1864
 0356 1865
 0356 1866
 0356 1867
 0356 1868
 0356 1869
 58 07FF 8F BB 0356 1870 PUSHR #^M<R0,R1,R2,R3,R4,R5,R6,R7,R8,R9,R10> :
 58 000D'CF DE 035A 1871 MOVAL W^MBATAB,R8 : GET MBA TABLE OF CONSTANTS
 59 0000'CF 9E 035F 1872 MOVAB W^MBASINT,R9 : ADDRESS OF INTERRUPT SERVICE ROUTINE
 5A 0000'CF 9E 0364 1873 MOVAB W^MBASINITIAL,R10 : ADDRESS OF DEVICE INITIALIZATION
 0369 1874 :10\$: :
 0369 1875 :+ Allocate and initialize Channel Request Block.
 51 0048 8F 3C 0369 1876 :
 B6 10 036E 1877 :
 0369 1878 :
 0369 1879 :
 0369 1880 : MOVZWL #CRBSC LENGTH,R1 : SET SIZE OF CRB
 036E 1881 : BSBBL ALONPAGD : ALLOCATE SPACE FOR CRB

08 A2 51 B0 0370 1882
0A A2 05 90 0374 1883
04 A2 62 62 DE 0378 1884
50 24 A2 9E 037F 1885
80 9F 163CBB 8F 00 0383 1886
80 59 00 038A 1887
60 80 D4 038D 1888
5A 52 00 038F 1889
5A 52 00 0392 1890
5A 52 00 0395 1891
51 00000038 9F41 68 9A 0395 1892
08 A2 51 B0 03A2 1893
0A A2 09 90 03A6 1894
62 00E4'CF44 0C A2 68 98 03AA 1895
2C AA 52 00 0384 1896
59 52 00 0388 1897
51 01 A8 3C 0388 1898
FF64 30 03BF 1899
08 A2 51 B0 03C2 1900
0A A2 01 90 03C6 1901
62 69 00 03CA 1902
0C A2 54 B0 03CD 1903
03 A8 98 03D1 1904
0E A2 00 03D4 1905
10 A2 5A 00 03D6 1906
03DA 1907
03DA 1908
03DA 1909
03DA 1910
50 00000000'GF 00 03DA 1911
55 5B 09 78 03E1 1912
50 55 C0 03E5 1913
54 54 04 00 EF 03E8 1914
50 0100 C044 DE 03ED 1915
1C A2 50 DO 03F3 1916
60 25 AA DE 03F7 1917
40 A0 25 AA DE 03FB 1918
0080 C0 25 AA DE 0400 1919
00C0 C0 25 AA DE 0406 1920
040C 1921
040C 1922
040C 1923
040C 1924
50 00000000'GF 00 03DA 1925
55 5B 09 78 03E1 1926
50 55 C0 03E5 1927
54 54 04 00 EF 03E8 1928
50 0100 C044 DE 03ED 1929
1C A2 50 DO 03F3 1930
60 25 AA DE 03F7 1931
40 A0 25 AA DE 03FB 1932
0080 C0 25 AA DE 0400 1933
00C0 C0 25 AA DE 0406 1934
040C 1935
040C 1936
040C 1937
14 A2 25 AA DE 040C 1938

MOVW R1,CRBSW_SIZE(R2) : SET CORRECT SIZE
MOVB #DYNSC_CRB,CRBSB_TYPE(R2) : SET CORRECT TYPE
MOVAL CRBSL_WQFL(R2),CRBSL_WQFL(R2) : INITIALIZE WAIT QUEUE HEADER
MOVAL CRBSL_WQFL(R2),CRBSL_WQBL(R2) : FLINK AND BLINK
MOVAB CRBSL_INTD(R2),R0 : SET ADDRESS OF INTD AREA
MOVL #X9FT63CBB,(R0) : "PUSHR MCR2 R3,R4,R5> JSB 24"
MOVL R9,(R0) : ADDR OF XXXSINT ROUTINE
CLRL (R0) : CLEAR OUT UNNEEDED AREA
MOVL R10,(R0) : ADDR OF XXXSINITIAL ROUTINE
MOVL R2,R10 : SAVE CRB ADDRESS

MOVZBL ADPTAB_IDBUNITS(R8),R1 : GET # OF IDB UNITS
MOVAL #IDB\$C_LENGTH[R1],R1 : GET TOTAL SIZE OF IDB
BSBB ALONPAGD : ALLOCATE SPACE FOR CRB
MOVW R1,IDBSW_SIZE(R2) : SET STRUCTURE SIZE
MOVB #DYNSC_IDB,- : AND TYPE CODE
IDBSB_TYPE(R2) :
MOVZBW ADPTAB_IDBUNITS(R8),- : SET COUNT OF UNITS
IDBSW_UNITS(R2) :
MOVL W\$BICONF[R4],- : SET CSR ADDRESS TO
IDBSL_CSR(R2) : START OF ADAPTER REG SPACE
MOVL R2,- : SET ADDRESS OF IDB INTO CRB
MOVL CRBSL_INTD+VECSL_IDB(R10) :
MOVL R2,R9 : SAVE ADDRESS OF IDB

MOVZBL ADPTAB_ADPLEN(R8),R1 : GET SIZE OF ADAPTER
BSBW ALONPAGD : ALLOCATE SPACE FOR CRB
MOVW R1,ADPSW_SIZE(R2) : SET SIZE OF STRUCTURE
MOVB #DYNSC_ADP,ADPSB_TYPE(R2),- : AND TYPE CODE
IDBSL_CSR(R9),ADPSL_CSR(R2) : SET ADDRESS OF CONFIGURATION REGISTER
R4,ADPSW_TR(R2) : SET TR/SLOT-16 NUMBER OF ADAPTER
MOVZBW ADPTAB_ATYPE(R8),- : SET THE ADAPTER TYPE
ADPSW_APDTYPE(R2) :
MOVL R10,ADPSL_CRB(R2) : POINT ADP TO CRB
CMPW ADPSW_APDTYPE(R2),#ATS_CI : CI?
BEQL 20S : YES, DO NOT CONNECT UP VECTORS

MOVW G\$EXE\$GL_SCB,R0 : GET ADDRESS OF SCB
ASHL #9,R11,R5 : Turn SCB page offset into byte offset.
ADDL R5,R0 : set to beginning of correct SCB page.
EXTZV #0 #4 R4 R4 : Use low 4 bits of nexus number.
MOVAL ^X100{R0\$[R4]},R0 : COMPUTE ADDR OF 1ST VECTOR
MOVL R0,ADPSL_AVECTOR(R2) : SAVE ADDR OF ADAPTER'S SCB VECTORS
MOVAL CRBSL_INTD+1(R10),(R0) : CONNECT VECTOR TO CRB CODE
MOVAL CRBSL_INTD+1(R10),64(R0) : SAME FOR
MOVAL CRBSL_INTD+1(R10),128(R0) : ALL FOUR
MOVAL CRBSL_INTD+1(R10),192(R0) : VECTORS

20S: MOVAL CRBSL_INTD+1(R10),- : Continue with ADP initialization.
MOVAL CRBSL_INTD+1(R10),- : SAVE SCB VECTOR CONTENTS IN ADP

55 52	0C 52	88 0411	0411 1939	PUSHR #^M<R2,R3>	ADPSL MBASCB(R2)	SAVE SOME REGISTERS
52	62	DO 0413	1940 1941	MOVL R2,R5	ADPSL CSR(R2),R2	COPY ADP ADDRESS
00000000 GF	16	DO 0416	1942 1943	MOVL ADPSL_GMMG\$SVAPTECHK	VIRTUAL ADDRESS OF ADAPTER	
18 A5	63	DO 041F	1944 1945	JSB G^MMG\$SVAPTECHK	ADDRESS OF SPTE THAT MAPS ADAPTER	
38 AA	52	BA 0423	1945 1946	MOVL (R3) ADPSL_MBASPTE(R5)	SAVE CONTENTS OF SPTE	
14 A9	52	DO 0425	1946 1947	POPR #^M<R2,R3>	RESTORE REGISTERS	
FB00	30	DO 0429	1947 1948	MOVL R2,CRBSL_INTD+VECSL_ADP(R10)	SET CRB POINTER TO ADP	
		0430	1948 1949	MOVL R2,IBDSL_ADP(R9)	AND INTO IDB	
		0430	1949 1950	BSBW ADPLINK	LINK ADP TO END OF CHAIN	
		0430	1950 1951	; Initialize adapter hardware.		
55 54	59 65	DO 0430	1952 1953	MOVL R9,R5	ADDSL CSR(R5),R4	ADDRESS OF IDB
30 07FF	BA 8F	DO 0433	1953 1954	MOVL IDDSL_CSR(R5),R4	ADDSL_CONFIGURATION REGISTER 0	
	16	16 0436	1954 1955	JSB ACRB\$C_INTD+VECSL_INITIAL(R10)	INIT ADAPTER	
	05	BA 0439	1955 1956	POPR #^M<R0,R1,R2,R3,R4,R5,R6,R7,R8,R9,R10>	RESTORE ALL REGISTERS	
		043D	1956 1957	RSB	; RETURN	
		043E	1957 1958	.DSABL LSB		

043E 1997 .SBTTL INISKDZ11
043E 1998 ;++
043E 1999 : INPUTS:
043E 2000 R2 - VA of next free system page
043E 2001 R3 - VA of system page table entry to be used to map VA in R2
043E 2002 R4 - nexus identification number of this adapter
043E 2003
043E 2004
043E 2005 : OUTPUTS:
043E 2006
043E 2007 :--
043E 2008
043E 2009 INISKDZ11:
043E 2010
05 043E 2029 RSB ; Return to caller.

043F 2031 .SBTTL INISCONSOLE, init data structures for console
 043F 2032 ++
 043F 2033 FUNCTIONAL DESCRIPTION:
 043F 2034
 043F 2035 This routine is executed only once, during system initialization.
 043F 2036 It initializes the CRB and IDB for boot/console device.
 043F 2037
 043F 2038
 043F 2039
 043F 2040
 043F 2041
 043F 2042
 043F 2043
 043F 2044
 043F 2045
 043F 2046
 043F 2047
 043F 2048
 043F 2049
 043F 2050 ;--
 043F 2051
 043F 2052 INISCONSOLE::
 043F 2053 .ENABL LSB
 66 A6 91 043F 2054
 40 8F 0442 2056 CMPB RPBSB_DEVTYP(R6),- : BOOTING FROM CONSOLE BLOCK
 10 12 0444 2057 #BTDSR CONSOLE : STORAGE DEVICE?
 41534303 8F 00 0446 2058 BNEQ BLD_CRB : NO
 14 A3 044C 2059 MOVL #^A7(CSA/08+3,- : YES, SET DEVICE NAME
 044E 2060 DDBST_NAME(R3) : COUNTED STRING
 044E 2062
 54 A5 57 D4 044E 2067
 01 B0 0450 2070 CLRL R7 : CLEAR ADP POINTER
 0D 11 0454 2071 MOVW #1,UCBSW_UNIT(R5) : SET UNIT NUMBER TO 1
 0456 2072 BRB FILL_CRB
 0456 2075
 0456 2076
 0456 2077 ; NOW BUILD THE AUXILIARY DATA BLOCKS (CRB, IDB)
 0456 2078
 58 10 A7 D0 0456 2079 BLD_CRB:
 0E A7 01 B1 045A 2080 MOVL ADPSL_CRB(R7),RB : GET ADDRESS OF CRB IF IT EXISTS
 03 13 045E 2081 CMPW #ATS_OBA,ADPSW_ADPTYPE(R7) : IS THIS A UNIBUS ADAPTER?
 008A 31 0460 2082 BEQL FILL_CRB : YES, ALLOCATE CRB
 0463 2083 BRW 100\$: NO, CRB/IDB ALREADY ALLOCATED
 24 A2 00000000'9F 16 0463 2084
 9F 163FBB 8F 00 0469 2085 FILL_CRB:
 0471 2086 JSB #INISALLOC_CRB : GO ALLOCATE AND SETUP CRB
 0471 2087 MOVL #^X9F163FBB,CRBSL_INTD(R2) : SET PUSHR #^M<R0..,R5>
 38 A2 57 D0 0471 2088 ; JSB AND INTO INTERRUPT DISPATCH
 58 52 00 0475 2089 MOVL R7,CRBSL_INTD+VECSL_ADP(R2) : SET PTR TO ADP
 51 0058 8F 3C 0478 2090 MOVL R2,R8 : SAVE CRB POINTER
 00000000'9F 16 047D 2091 MOVZWL #<IDBSC_LENGTH+<8=4>>,R1 : SIZE TO ALLOCATE FOR IDB
 08 A2 51 B0 0483 2092 JSB #INISACONONPAGED : ALLOCATE IDB
 0A A2 09 90 0487 2093 MOVW R1,UCBSW_SIZE(R2) : SET SIZE OF IDB
 2C A8 52 D0 048B 2094 MOVB #DYNSC_IDB,UCBSW_TYPE(R2) : AND STRUCTURE TYPE CODE
 048F 2095 MOVL R2,CRBSL_INTD+VECSL_IDB(R8) : SET IDB INTO CRB
 66 A6 91 048F 2096
 048F 2099 CMPB RPBSB_DEVTYP(R6),- : BOOTING FROM CONSOLE BLOCK

50	000000F0 8F	00000000'9F	40 8F 26	0492 2100	BNEQ 10\$	#BTDSK_CONSOLE	; STORAGE DEVICE?
			80 25 A8	0494 2101	ADDL3	0#EXESGL SCB, #^XF0, R0	; NO
			60 49 A8	0496 2102	MOVAL	CRBSL_INTD+1(R8), (R0)+	; YES, GET ADDRESS OF VECTOR IN SCB
48 A8	9F163FBB 8F		04A2 2103	04A6 2104	MOVAL	CRBSL_INTD2+1(R8), (R0)	; SET ADDR IN 1ST VECTOR
			04AA 2105	04B2 2106	MOVL	#^X9FT63FBB, CRBSL_INTD2(R8)	; SET ADDR IN 2ND VECTOR
			50 A8 52	04B2 2107	MOVL	R2, CRBSL_INTD2+VECSL_IDB(R8)	; STORE PUSHR #^M<R0...R5>
			2C B8 1F	04B6 2108	MOVL	#P8S_CSTD, -	; JMP ON IN 2ND INT. DISPATCH
			04BA 2109	04BA 2110	BRB	ACRBSL_INTD+8(R8)	; STORE ADDRESS OF IDB IN CRB
			31 11	04BA 2111	100\$	100\$; STORE IPR NUMBER OF CONSOLE INTERFACE
			04BC 2113				; REGISTER AS DEVICE CSR ADDRESS
62	58 A6	00000000'9F	00 04BC 2114	10\$:	MOVL	RPBSL_CSRVIR(R6), -	; SAVE BOOT DEVICE CSR ADDRESS
			04C0 2115			IDBSL_CSR(R2)	; IN INTERRUPT DISPATCH BLOCK
			11 91 04C0 2116		CMPB	#BTDSR_UDA, -	; LOW ORDER BYTE OF ORIGINAL R0 TELLS
			66 A6 04C2 2117			RPBSB_DEVTYPE(R6)	; BOOT DEVICE TYPE.
			08 12 04C4 2118		BNEQ	20\$; IF NOT BOOTING FROM A UDA BRANCH
			04C6 2119		MOVL	RPBSL_CSRVIR(R6), -	; AROUND.
			04CE 2120			#^B00\$GB_SYSTEMID	; COPY VIRTUAL ADDRESS OF UDA PORT CSR
			04CE 2121				; TO LOW ORDER LONGWORD OF SYSTEMID
			04CE 2122	20\$:	MOVL	R7, IDBSL_AD(P2)	; POINT IDB TO ADP
14 A2 57	DO	04CE 2123			MOVZWL	RPBSW_R00BVEC(R6), R0	; GET USER SPECIFIED VECTOR
50 1E A6	3C	04D2 2124			BNEQ	30\$; BRANCH IF VECTOR SPECIFIED
		0A 12 04D6 2125			MOVZBL	RPBSB_DEVTYPE(R6), R0	; ELSE GET DEVICE TYPE CODE
50	50 66 A6	9A 04D8 2126			MOVZWL	W^BOOTVECTOR-2[R6], R0	; GET DEFAULT INTERRUPT VECTOR
50	FFE'CF40	3C 04DC 2127			MOVAB	BADPSL_VECTOR(R7)[R0], R0	; COMPUTE ADDRESS OF VECTOR
50	10 B740	9E 04E2 2128		30\$:	MOVAB	CRBSL_INTD+2(R8), (R0)	; SET ADDR OF INTERRUPT VECTOR
60	26 A8	9E 04E7 2129			DECL	(R0)	; BACK TWO BYTES TO PUSHR, +1 TO
		04EB 2130					
		60 D7 04EB 2133					
		04ED 2136					
		04ED 2137	100\$:		RSB		; RETURN
		04EE 2138					
		04EE 2139					

04EE 2141 .SBTTL EXESINI_TIMWAIT - COMPUTE CORRECT TIMEWAIT LOOP VALUES

04EE 2142 ++ FUNCTIONAL DESCRIPTION:

04EE 2143 EXESINI_TIMWAIT initializes EXESGL_TENUSEC and EXESGL_UBDELAY, cells used
04EE 2144 in the Time-wait macros. The first data cell, EXESGL_TENUSEC, is the number
04EE 2145 of times the following loop will be executed in ten u-seconds. This is
04EE 2146 done once here to calibrate the loop instead of reading the processor clock.
04EE 2147 The resulting number is used in the system macros TIMEWAIT and TIMEDWAIT.

04EE 2148 04EE 2149 04EE 2150 04EE 2151 04EE 2152 04EE 2153 04EE 2154 04EE 2155 04EE 2156 04EE 2157 04EE 2158 04EE 2159 04EE 2160 04EE 2161 04EE 2162 04EE 2163 04EE 2164 04EE 2165 04EE 2166 04EE 2167 04EE 2168 04EE 2169 04EE 2170 04EE 2171 04EE 2172 04EE 2173 04EE 2174 04EE 2175 04EE 2176 04EE 2177 04EE 2178 04EE 2179 04EE 2180 04EE 2181 04EE 2182 04EE 2184 04EE 2185 04EE 2189 04F1 2191 04F1 2193 04F1 2197 04F1 2202 04F1 2203 04F8 2204 04FB 2205 04FB 2206 04FB 2207 04FB 2208 04FB 2209 04FB 2213

++
EXESINI_TIMWAIT initializes EXESGL_TENUSEC and EXESGL_UBDELAY, cells used
in the Time-wait macros. The first data cell, EXESGL_TENUSEC, is the number
of times the following loop will be executed in ten u-seconds. This is
done once here to calibrate the loop instead of reading the processor clock.
The resulting number is used in the system macros TIMEWAIT and TIMEDWAIT.

04EE 2150 The first step is to initialize EXESGL_UBDELAY. If the bit test instruction
04EE 2151 in the TIMEWAIT macro is executed too rapidly in a loop, it can saturate the
04EE 2152 Unibus. EXESGL_UBDELAY is used to introduce a 3 microsecond delay loop into
04EE 2153 the TIMEWAIT bit test loop.

04EE 2154 This routine is called only once, from INIT.

04EE 2155 INPUT PARAMETERS:

04EE 2156 NONE

04EE 2157 IMPLICIT INPUTS:

04EE 2158 Time-of-day processor clock.
04EE 2159 Interval timers.

04EE 2160 OUTPUT PARAMETERS:

04EE 2161 R0 - Destroyed.

04EE 2162 IMPLICIT OUTPUTS:

04EE 2163 EXESGL_TENUSEC - set to appropriate value to make TIMEWAIT and TIMEDWAIT
04EE 2164 macros loop for 10 micro-seconds.

04EE 2165 EXESGL_UBDELAY - set to appropriate value to make TIMEWAIT and TIMEDWAIT
04EE 2166 macros loop for 3 micro-seconds in the unibus delay
04EE 2167 loop.

04EE 2168 04EE 2169 04EE 2170 04EE 2171 04EE 2172 04EE 2173 04EE 2174 04EE 2175 04EE 2176 04EE 2177 04EE 2178 04EE 2179 04EE 2180 04EE 2181 04EE 2182 04EE 2184 04EE 2185 04EE 2189 04F1 2191 04F1 2193 04F1 2197 04F1 2202 04F1 2203 04F8 2204 04FB 2205 04FB 2206 04FB 2207 04FB 2208 04FB 2209 04FB 2213

04EE 2182 EXESINI_TIMWAIT:: : Initialize time-wait data cells
04EE 2184 .ENABLE LSB

19 00 DA 04EE 2189 MTPR #0,#PR7508_NICR : Initialize next interval count register.

7E 00004E20 8F 18 11 DA 04F1 2203 MOVL #20000,-(SP)
04F8 2204 MTPR #^X11,#PR8_ICCS : # of times to execute timed loop.
04FB 2205 : Start clock, no interrupts.

FD 6E FS 04FB 2206 : * * * start of loop to time * * *
04FB 2207 10\$: SOBGTR (SP),10\$: Delay loop.
04FB 2208 : * * * end of loop to time * * *
04FB 2209
04FB 2213

0556 2299 .SBTTL EXESINIT_TODR - SET SYSTEM TIME TO CORRECT VALUE AT STARTUP

0556 2300 :++ FUNCTIONAL DESCRIPTION:

0556 2301
0556 2302
0556 2303
0556 2304
0556 2305
0556 2306
0556 2307
0556 2308
0556 2309
0556 2310
0556 2311
0556 2312
0556 2313
0556 2314
0556 2315
0556 2316
0556 2317
0556 2318
0556 2319
0556 2320
0556 2321
0556 2322
0556 2323
0556 2324
0556 2325
0556 2326
0556 2327
0556 2328
0556 2329
0556 2330
0556 2331
0556 2332
0556 2333
0556 2334
0556 2335
0556 2336
0556 2337
0556 2338
0556 2339
0556 2340
0556 2341
0556 2342
0556 2343
0556 2344
0556 2345
0556 2346
0556 2347
0556 2348
0556 2349
0556 2350
0556 2351
0556 2352
0556 2353
0556 2354

EXESINIT_TODR SOLICITS THE CORRECT TIME FROM THE OPERATOR IF NECESSARY. CONVERTS THE ASCII RESPONSE TO BINARY FORMAT AND CALLS AN INTERNAL ENTRY POINT OF THE SSETIME SYSTEM SERVICE TO SET THE NEW SYSTEM TIME IN MEMORY WITHOUT MODIFYING THE CONTENTS OF THE SYSTEM DISK.

IF THE TIME WOULD NORMALLY BE SOLICITED FROM AN OPERATOR, BECAUSE THE HARDWARE TIME OF YEAR CLOCK IS ZERO, THEN THE SYSGEN PARAMETER "TPWAIT" IS CHECKED. IF IT IS ZERO, THEN IT IS ASSUMED THAT NO OPERATOR IS PRESENT AND THE SYSTEM IS BOOTTED USING THE LAST TIME RECORDED IN THE SYSTEM IMAGE. IF THE PARAMETER IS NON ZERO THEN THAT TIME IS USED AS THE MAXIMUM TIME TO WAIT BEFORE ASSUMING THAT THERE IS NO OPERATOR AND BOOTING ANY WAY. IF THE PARAMETER IS NEGATIVE, THE SYSTEM WILL WAIT FOREVER.

THIS ROUTINE IS CALLED ONLY ONCE, FROM SYSINIT OR STASYSGEN.

INPUT PARAMETERS:

NONE

IMPLICIT INPUTS:

TIME-OF-DAY PROCESSOR CLOCK.

OUTPUT PARAMETERS:

R0,R1 - DESTROYED

IMPLICIT OUTPUTS:

EXESGQ_SYS TIME - SET TO CURRENT TIME IN 100 NANOSECOND UNITS SINCE 17-NOV-1858 00:00:00.

Stack storage offsets:

00000000 0556
00000004 0556
0000000C 0556
00000014 0556
0000001C 0556
00000014 0556

: CHANNEL FOR TERMINAL (LONGWORD)
: STRING DESCRIPTOR FOR OPERATOR'S TERM
: TEMPORARY STRING DESCRIPTOR (QUADWORD)
: INPUT TIME VALUE (QUADWORD)
: INPUT LINE BUFFER (5 LONGWORDS)
: (LENGTH OF LINE BUFFER IN BYTES)

PURE DATA

TERM_NAMADR:

: DEVICE NAME FOR OPERATOR'S TERMINAL

.ASCII \OPA0\
TERM_NAMSZ = - TERM_NAMADR
TIMERR: .ASCII \invalid date/time\

30 41 50 4F
00000004 055A
74 61 64 20 64 69 6C 61 76 6E 69 00
65 60 69 74 2F 65 0566

54 4E 45 20 65 53 61 45 4C 50 0A 00 11 055A
20 44 4E 41 20 45 54 41 44 20 52 45 33 056C
4D 4D 4D 20 44 44 28 20 45 4D 49 54 0579
4D 4D 3A 48 48 20 20 59 59 59 59 20 0585
20 20 29 0591
00000033 059D 05A0 2355 TIMEPROMPT:
05A0 2356 .BYTE NPROMPT
05A0 2357 .ASCII <13><10>/PLEASE ENTER DATE AND TIME (DD-MMM-YYYY HH:MM) /
05A0 2358 NPROMPT=-TIMEPROMPT-1
05A0 2359
05A0 2360
05A0 2361 EXESINIT_TODR:: : SET CORRECT TIME
077C 8F BB 05A0 2362 .ENABLE LSB
SE 30 C2 05A4 2363 PUSHR #^M<R2,R3,R4,R5,R6,R8,R9,R10> : SAVE REGISTERS
56 5E D0 05A7 2364 SUBL #4*12,SP : SCRATCH STORAGE
04 A6 04 9A 05AA 2365 MOVL SP,R6 : SAVE ADDRESS OF SCRATCH STORAGE
08 A6 FFA4 CF 9E 05AE 2366 MOVZBL #TERM_NAMSIZ,TTNAME(R6) : SET SIZE OF OPERATOR'S TERM NAME AND
1C 00000000'GF 00' E0 05B4 2367 MOVAB W^TERM_NAMADR TTNAME+4(R6) : PIC ADDRESS INTO TERM NAME DESC
05BC 2368 BBS S^EXESV_SETTIME,G^EXESGL_FLAGS,RFADTIME : BR TO SOLICIT TIME
05BC 2369
05BC 2370
05BC 2374
50 1B DB 05BC 2376 MFPR #PR750\$_TODR,RO : GET TIME OF DAY CLOCK VALUE
05BF 2378
05BF 2382
59 00000000'GF 50 C3 05BF 2386
09 1B 05C7 2388
0083D600 8F 59 D1 05C9 2389 SUBL3 R0,G^EXESGL_TODR,R9 : GET TOD DELTA TIME (10 MS UNITS)
06 1E 05D0 2390 BLEQU 5\$: BRANCH IF TIME IS LATER
14 A6 7C 05D2 2391 CMPL R9,#24*60*60*100 : CHECK FOR SETBACK OF ONE DAY
00C7 31 05D5 2396 5\$: BGEQU READTIME : MORE, MUST SOLICIT TIME
05D8 2397 CLRQ INTIME(R6) : NULL ARGUMENT FOR EXESSETIME_INT
05D8 2398 BRW 200\$: RETURN TO CALLER
58 00000000'GF 59 D4 05D8 2399 READTIME: : SOLICIT TIME
32 05DA 2400 CLRQ R9 : CLEAR A FLAG
14 14 05E1 2401 CVTWL G^SGNSGW_TPWAIT,R8 : PICK UP TIMEOUT WAIT INTERVAL
0D 19 05E3 2402 BGTR 8\$: POSITIVE, WAIT THAT PERIOD ONCE
BLSS 7\$: NEGATIVE IS WAIT FOREVER
50 00000000'GF 01 C1 05E5 2404 6\$: ADDL3 #1,G^EXESGL_TODR,RO : ZERO, SET TIME-OF-DAY CLOCK TO
05ED 2406
1B 50 DA 05ED 2414 MTPR R0,#PR750\$_TODR : KNOWN VALUE + 10 MSEC AND FINISH UP
05F0 2416
05F0 2420
E0 11 05F0 2424
05F2 2426
05F2 2428
58 14 D0 05F2 2434 7\$: MOVL #20,R8 : STARTING WAIT
59 D6 05F5 2435 INCL R9 : NEGATIVE - WAIT FOREVER
05F7 2436 8\$: \$ASSIGN_S TTNAME(R6),TTCHAN(R6) : AND ASSIGN TO INPUT DEVICE
52 DD 50 E9 0605 2437 BLBC R0,6\$: ERROR - FALL BACK TO STORED TIME
FF60 CF 9E 0608 2438 10\$: MOVAB W^TIMEPROMPT,R2 : GET ADDRESS OF PROMPT STRING
53 82 9A 060D 2439 MOVZBL (R2)+R3 : AND LENGTH
0610 2440 SQIOW_S #0,W^TTCHAN(R6),- : PROMPT AND READ TIME
0610 2441 #<IOS_READPROMPT!IOSM_PURGE!IOSM_TIMED!IOSM_CVTLow>,-

06BB 2486 DEAL_INIT_CODE: ; DEALLOCATE THE INITIALIZATION CODE

06BB 2487 :
06BB 2488 : It is the duty of the last-executed, loadable initialization
06BB 2489 : routine to make itself and all other such routines disappear, i.e.,
06BB 2490 : release the space they occupy to non-paged pool. Each routine's vector
06BB 2491 : must be disconnected, e.g., be made to point to the symbol, EXESLOAD_ERROR.
06BB 2492 :
06BB 2493 : NOTE: This means that new initialization routines should be added
06BB 2494 : to this module in a particular order, not necessarily at the
06BB 2495 : end of the module!
06BB 2496 :
06BB 2497 :
7E 52 7D 06BB 2498 .ENABLE LSB
06BE 2499 MOVO R2,-(SP) : Save some registers

06BE 2500 :
06BE 2501 : First find the vectors that point to these initialization routines
06BE 2502 : and reset them to point to EXESLOAD_ERROR.
06BE 2503 :
51 50 0000'CF 9E 06BF 2504 :
52 00000000'8F C1 06C3 2505 :
53 00000000'GF 9E 06CB 2506 :
9F17 8F 62 B1 06D9 2507 :
18 13 06DE 2508 10\$:
80 8F 03 A2 91 06E0 2510 :
16 12 06E5 2511 :
50 62 01 06E7 2512 :
0C 1F 06EA 2513 :
51 62 01 06EC 2514 :
07 1A 06EF 2515 :
62 00000000'GF 9E 06F1 2516 :
52 02 C0 06F8 2517 20\$:
52 06 06FB 2518 30\$:
52 06 06FD 2519 40\$:
53 52 01 06FF 2520 :
D5 1F 0702 2521 :
0704 2522 :
0704 2523 : Now release the memory to non-paged pool.
0704 2524 :
50 0000'CF 9E 0704 2525 :
51 0000'8F 3C 0709 2526 :
F8FB' 31 070E 2527 :
0711 2528 :
00000000 2529 :
0000 2530 :
0000 2531 STAY_HEADER:
00000000 00000000 0000 2532 :
0000 0008 2533 :
62 000A 2534 :
00 000B 2535 :
000C 2536 :
00000000'9F 16 000C 2537 50\$:
52 8E 7D 0012 2538 :
05 0015 2539 :
0016 2540 :
0016 2541 :
0016 2542 :
MOVAB W\$SYSLSBEGIN, R0 : Compute bounds of releasable piece:
ADDL3 #<STAY_HEADER-SYSL\$BEGIN>, R0, R1 ; starting and ending addresses.
MOVAB G\$EXES\$LOADVEC, R2 : Get starting address of vectors.
MOVAB G\$EXES\$LOAD_ERROR, R3 : Get end of vectors.
CMPW (R2), #^X9FT? : Is this JMP 3# ?
BEQL 30\$: Br if yes, skip past it.
CMPB 3(R2), #^X80 : Is this a system space address
BNEQ 40\$: Br if no, assume it's a HALT instr.
CMPL (R2), R0 : Is address before the releasable
BLSSU 20\$: piece of memory? Br on yes.
CMPL (R2), R1 : Is address after the releasable
BGTRU 20\$: piece of memory? Br on yes.
MOVAB G\$EXES\$LOAD_ERROR, (R2) : Reset this vector.
ADDL #2, R2 : Point past this vector.
INCL R2 : Come here to point past JMP 3#.
INCL R2 : Come here to point past HALT.
CMPL R2, R3 : Past the end of the vectors?
BLSSU 10\$: Keep searching vectors.

0704 2525 :
MOVAB W\$SYSLSBEGIN, R0 : Point to start of module
MOVZWL #<STAY_HEADER-SYSL\$BEGIN>, R1 ; Length to vaporize
BRW 50\$: Br to code that is not released.

.PSECT \$SSINIT__END.PAGE : 'PAGE' SINCE 16-BYTE ALIGN IS NOT

00000000 00000000 0000 2532 :
0000 0008 2533 :
62 000A 2534 :
00 000B 2535 :
000C 2536 :
.LONG 0, 0 :
.WORD <SYSL\$END-STAY_HEADER> :
.BYTE DYN\$C_LOADCODE :
.BYTE 0 :
JSB @EXES\$DEANONPGDSIZ : Just the smile on the Cheshire cat
MOVO (SP)+, R2 : Restore
RSB : Return.

.DISABLE LSB
.END

SSSVM\$DEFINED	=	00000001	CONFREGL	000001E4	R	08
SST1	=	00000001	CPU_ADP\$IZE	00000019	R	08
ADAPTERS	=	00000000 R 02	CPU_TYPE	= 00000002		
ADP\$B_TYPE	=	0000000A	CR	= 0000000D		
ADP\$C_CIADP\$LEN	=	00000030	CRBSB_TYPE	= 0000000A		
ADP\$C_DRADP\$LEN	=	00000030	CRBSC_LENGTH	= 00000048		
ADP\$C_MBAADP\$LEN	=	00000030	CRBSL_INTD	= 00000024		
ADP\$C_UBAADP\$LEN	=	00000258	CRBSL_INTD2	= 00000048		
ADP\$L_AVECTOR	=	0000001C	CRBSL_WQBL	= 00000004		
ADP\$L_CRB	=	00000010	CRBSL_WQFL	= 00000000		
ADP\$L_CSR	=	00000000	CRBSW_SIZE	= 00000008		
ADP\$L_DPQFL	=	00000014	CREATE ARRAYS	0000011A	R	09
ADP\$L_LINK	=	00000004	CSR_LEN_OFFSET	= FFFFFFFB		
ADP\$L_MBASCB	=	00000014	DBB\$T_NAME	= 00000014		
ADP\$L_MBASPT	=	00000018	DEAL_INIT_CODE	00000688	R	09
ADP\$L_MRACTMDRS	=	0000005C	DIRECT_VEC_NODE_CNT	00000009	R	08
ADP\$L_MRQFL	=	00000030	DRSINITIAL	*****	X	09
ADP\$L_UBASCB	=	00000044	DRSINT	*****	X	09
ADP\$L_UBASPT	=	00000054	DRTAB	00000011	R	08
ADP\$L_VECTOR	=	00000010	DYN\$C_APP	= 00000001		
ADP\$W_ADP\$TYPE	=	0000000E	DYN\$C_CONF	= 00000007		
ADP\$W_DPBITMAP	=	00000060	DYN\$C_CRB	= 00000005		
ADP\$W_MRFENCE	=	0000015C	DYN\$C_IDB	= 00000009		
ADP\$W_MRFREGARY	=	0000015E	DYN\$C_INIT	= 00000063		
ADP\$W_MRNFENCE	=	00000062	DYN\$C_LOADCODE	= 00000062		
ADP\$W_MRNRREGARY	=	00000064	END_NEXUS	00000115	R	09
ADP\$W_SIZE	=	00000008	ERROR_HALT	00000199	R	09
ADP\$W_TR	=	0000000C	ERROR_HALT_1	0000019E	R	09
ADP\$W_UMR_DIS	=	00000256	EXES\$AL_LOAD\$C	*****	X	09
ADPLINK	*****	X 09	EXES\$DE\$NONPGD\$SIZ	*****	X	0A
ADPTAB_ADP\$LEN	=	00000001	EXES\$GL_CONFREGL	*****	X	09
ADPTAB_ATYPE	=	00000003	EXES\$GL_FLAGS	*****	X	09
ADPTAB_IDB\$UNITS	=	00000000	EXES\$GL_NUMNEXUS	*****	X	09
ALONPAGD	=	00000326 R 09	EXES\$GL_RPB	*****	X	09
ATS_CI	=	00000004	EXES\$GL_SCB	*****	X	09
ATS_DR	=	00000002	EXES\$GL_TENUSEC	*****	X	09
ATS_MBA	=	00000000	EXES\$GL_TODR	*****	X	09
ATS_UBA	=	00000001	EXES\$GL_UBDELAY	*****	X	09
BAD\$MR	=	0000030D R 08	EXES\$GQ_BOOTTIME	*****	X	09
BI_BUS_CODE	=	80000000	EXES\$GQ_TODCBASE	*****	X	09
BI_CPU	=	00000000	EXES\$INIT_TODR	000005A0	RG	09
BI_CSR_LEN	=	00000002	EXES\$INI_TIMWAIT	000004EE	RG	09
BI_LIKE	=	00000000	EXES\$LOAD_ERROR	*****	X	09
BLB_CRB	=	00000456 R 09	EXES\$MCHK_PRTCT	*****	X	09
BO0\$GB_SYSTEMID	*****	X 09	EXES\$OUTZ\$STRING	*****	X	09
BO0\$GL_SPTFREH	*****	X 09	EXES\$SETTIME_INT	*****	X	09
BO0\$GL_SPTFREL	*****	X 09	EXES\$TEST_CSR	*****	X	09
BOOTVECTOR	=	00000000 R 08	EXES\$UBAERR_INT	*****	X	09
BTDSK_CONSOLE	=	00000040	EXES\$V_SETTIME	*****	X	09
BTDSK_UDA	=	00000011	FILL_CRB	00000463	R	09
BUS_CODE_OFFSET	=	FFFFFFFFFFC	GET_GEN_TYPE	000000B9	R	09
BUS_CSRLEN	=	00000004 R 08	GET_TYPE	000000A0	R	09
CIS\$INITIAL	*****	X 09	IDBSB_TYPE	0000000A		
CIS\$INT	*****	X 09	IDBSC_LENGTH	00000038		
CITAB	=	00000015 R 08	IDBSL_APP	00000014		
CONFIG_IOSPACE	=	0000005F R 09	IDBSL_CSR	00000000		
CONFREG	=	000000A4 R 08				

IDBSW_SIZE	= 00000008	NDTS_MPM0	= 00000040
IDBSW_UNITS	= 0000000C	NDTS_MPM1	= 00000041
INISACLOC_CRB	***** X 09	NDTS_MPM2	= 00000042
INISALONONPAGED	***** X 09	NDTS_MPM3	= 00000043
INISCIADP	00000341 R 09	NDTS_SCORMEM	= 80000001
INISCONSOLE	0000043F RG 09	NDTS_UB0	= 00000028
INISDRADP	0000032C R 09	NDTS_UB1	= 00000029
INISIOMAP	00000000 RG 09	NDTS_UB2	= 0000002A
INISKDZ11	0000043E R 09	NDTS_UB3	= 0000002B
INISMBADP	00000356 R 09	NEXUSDESC	= 00000020 R 08
INISMPADP	***** X 06	NOSPT	= 000002E4 R 08
INISUBADP	000001C4 R 09	NPROMPT	= 00000033
INISUBSPACE	000001A7 R 09	NUMUBAVEC	= 00000080
INIT_ROUTINES	00000000 R 06	NUM_PAGES	= 00000000 R 04
INTIME	= 00000014	NXT_NEXUS	= 00000068 R 09
IOSM_CVLOW	***** X 09	PA	= 00F40000
IOSM_PURGE	***** X 09	PRS_CSTD	= 0000001F
IOSM_TIMED	***** X 09	PRS_ICCS	= 00000018
IOS_READPROMPT	***** X 09	PRS_SID_TYP730	= 00000003
IOS_WRITEVBLK	***** X 09	PRS_SID_TYP750	= 00000002
I0750\$AL_I0BASE	= 00F20000	PRS_SID_TYP780	= 00000001
I0750\$AL_PERNEX	= 00002000	PRS_SID_TYP790	= 00000004
I0750\$AL_UB0SP	= 00FC0000	PRS_SID_TYP8NN	= 00000006
LF	= 0000000A	PRS_SID_TYP8SS	= 00000005
LINBUF	= 0000001C	PRS_SID_TYPUV1	= 00000007
LINBUFSIZ	= 00000014	PRS_TB15	= 0000003A
MAP_NEXUS	000000F9 R 09	PR750\$_ICR	= 0000001A
MAP_PAGES	00000173 R 09	PR750\$_NICR	= 00000019
MAXNEXUS	= 00000040	PR750\$_TODR	= 0000001B
MBASINITIAL	***** X 09	PTESC_RW	= 10000000
MBASINT	***** X 09	PTESM_VALID	= 80000000
MBATAB	0000000D R 08	READTIME	= 000005D8 R 09
MCHKSM_LOG	= 00000001	RPBSB_DEVTYPE	= 00000066
MCHKSM_NEXM	= 00000004	RPBSL_ADPPHY	= 0000005C
MMGSGL_SBICONF	***** X 09	RPBSL_AdPVIR	= 00000060
MMGSGL_SPTBASE	***** X 09	RPBSL_BOOTR1	= 00000020
MMGSSVAPTECHK	***** X 09	RPBSL_CSRPHY	= 00000054
NDTS_BUA	= 80000102	RPBSL_CSRVIR	= 00000058
NDTS_CI	= 00000038	RPBSW_ROUBVEC	= 0000001E
NDTS_DR32	= 00000030	SBICONF	= 000000E4 R 08
NDTS_KDZ11	= 80000105	SBI_BUS_CODE	= 00000000
NDTS_MB	= 00000020	SBI_CPU	= 00000000
NDTS_MEM1664NI	= 00000012	SBI_CSR_LEN	= 00000001
NDTS_MEM16I	= 00000011	SBI_LIKE	= 00000001
NDTS_MEM16NI	= 00000010	SGNSGW_TPWAIT	***** X 09
NDTS_MEM256EIL	= 00000071	STAY_HEADER	= 00000000 R 0A
NDTS_MEM256EIU	= 00000073	SW_BUS_CODE	= 00000005 R 08
NDTS_MEM256I	= 00000074	SYSSASSIGN	***** GX 09
NDTS_MEM256NIL	= 00000070	SYSSBINTIM	***** GX 09
NDTS_MEM256NIU	= 00000072	SYSSDASSGN	***** GX 09
NDTS_MEM4I	= 00000009	SYSSQIOW	***** GX 09
NDTS_MEM4NI	= 00000008	SYSL\$BEGIN	***** X 09
NDTS_MEM64EIL	= 00000069	SYSL\$END	***** X 0A
NDTS_MEM64EIU	= 00000068	TERM_NAMADR	= 00000556 R 09
NDTS_MEM64I	= 0000006C	TERM_NAMSIZ	= 00000004
NDTS_MEM64NIL	= 00000068	TEST_NEXUS	= 00000071 R 09
NDTS_MEM64NIU	= 0000006A	TIMEPROMPT	= 0000056C R 09

```

TIMERR          0000055A R   09
TMPDESC
TTCHAN
TTNAME
UASSW IP CR1
UBASINITIAL
UBASINTO
UBASL MAP
UBASUREXINT
UBA1INT
UCBSW UNIT
VASM SYSTEM
VECSC_ADP
VECSL_IDB
VECSL_INITIAL
= 0000000C
= 00000000
= 00000004
= 00001464
***** X 09
***** X 09
= 00000800
***** X 09
0000031E R 09
= 00000054
= 80000000
= 00000014
= 00000008
= 0000000C

```

```

+-----+
! Psect synopsis !
+-----+

```

PSECT name	Allocation	PSECT No.	Attributes
. ABS .	00000000 (0.) 00 (0.)	NOPIC USR	CON ABS LCL NOSHR NOEXE NORD NOWRT NOVEC BYTE
\$ABSS	00000004 (4.) 01 (1.)	NOPIC USR	CON ABS LCL NOSHR EXE RD WRT NOVEC BYTE
\$\$SINITSDATA0	00000074 (116.) 02 (2.)	NOPIC USR	CON REL LCL NOSHR EXE RD WRT NOVEC BYTE
\$\$SINITSDATA1	00000000 (0.) 03 (3.)	NOPIC USR	CON REL LCL NOSHR EXE RD WRT NOVEC BYTE
\$\$SINITSDATA2	0000003A (58.) 04 (4.)	NOPIC USR	CON REL LCL NOSHR EXE RD WRT NOVEC BYTE
\$\$SINITSDATA3	00000000 (0.) 05 (5.)	NOPIC USR	CON REL LCL NOSHR EXE RD WRT NOVEC BYTE
\$\$SINITSDATA4	00000074 (116.) 06 (6.)	NOPIC USR	CON REL LCL NOSHR EXE RD WRT NOVEC BYTE
\$\$SINITSDATA5	00000000 (0.) 07 (7.)	NOPIC USR	CON REL LCL NOSHR EXE RD WRT NOVEC BYTE
\$\$SINITSDATA	0000033F (831.) 08 (8.)	NOPIC USR	CON REL LCL NOSHR EXE RD WRT NOVEC LONG
\$\$SINIT\$CODE	00000711 (1809.) 09 (9.)	NOPIC USR	CON REL LCL NOSHR EXE RD WRT NOVEC QUAD
\$\$SINIT__END	00000016 (22.) 0A (10.)	NOPIC USR	CON REL LCL NOSHR EXE RD WRT NOVEC PAGE

```

+-----+
! Performance indicators !
+-----+

```

Phase	Page faults	CPU Time	Elapsed Time
Initialization	29	00:00:00.04	00:00:02.08
Command processing	109	00:00:00.47	00:00:03.49
Pass 1	531	00:00:13.91	00:00:52.73
Symbol table sort	0	00:00:01.72	00:00:07.34
Pass 2	291	00:00:04.15	00:00:16.06
Symbol table output	29	00:00:00.15	00:00:00.40
Psect synopsis output	3	00:00:00.04	00:00:00.04
Cross-reference output	0	00:00:00.00	00:00:00.00
Assembler run totals	994	00:00:20.48	00:01:22.70

The working set limit was 2100 pages.

139241 bytes (272 pages) of virtual memory were used to buffer the intermediate code.

There were 90 pages of symbol table space allocated to hold 1656 non-local and 37 local symbols.

2546 source lines were read in Pass 1, producing 39 object records in Pass 2.

47 pages of virtual memory were used to define 45 macros.

! Macro library statistics !

Macro library name

\$255\$DUA28:[SYS.OBJ]LIB.MLB;1
-\$255\$DUA28:[SYSLIB]STARLET.MLB;2
TOTALS (all libraries)

Macros defined

23
14
37

1808 GETS were required to define 37 macros.

There were no errors, warnings or information messages.

MACRO/LIS=LISS:INIADP750/OBJ=OBJ\$:INIADP750 MSRC\$:CPUSW750/UPDATE=(ENH\$:(CPUSW750)+MSRC\$:INIADP/UPDATE=(ENH\$:(INIADP)+EXECML\$:/LIB

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